DOC NO.
930-600019-000

FROM THE ALLSTAR

TO THE

SUPERSTAR OEM BOARD

PART NUMBER 220-604061-xxx

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VERSION AND REVISION RECORD

VERSION	REVISION LETTER	DRA/SRA/SECO NO.	PAGES AFFECTED	DATE
000	-		Original Release	Jul/98
000	A	ECO98 - 0471	1,2	Jul/98
000	B	ECO00-1316	A, ii, 1-2	Sept/00
000	C	??????????	A, 1, 2	Aug/01

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1 INTRODUCTION

CMC Electronics Inc. referred hereafter as CMC is introducing the ***SUPERSTAR***: a breakthrough in low-cost and small-size superior quality GPS receivers for embedded applications. The ***SUPERSTAR*** is similar to the highly popular ***ALLSTAR*** high-end OEM Receiver and has kept the same robust signal tracking and unsurpassed tracking capability under FOLIAGE. The ***SUPERSTAR*** is the only low cost GPS OEM Receiver on the market offering sub-meter DGPS capability

The ***SUPERSTAR*** is a complete GPS OEM sensor that provides 3D navigation on a single compact board with full differential capability. The ***SUPERSTAR*** is a 12-channel GPS receiver that tracks all-in view satellites. It is fully autonomous in the sense that once power is applied, the ***SUPERSTAR*** automatically searches, acquires and tracks GPS satellites. When a sufficient number of satellites are tracked with valid measurements, the Superstar produces 3D position and velocity output with an associated figure of merit (FOM).

The ***SUPERSTAR*** has the same architecture than the ALLSTAR based on the GEC Plessey GPS chipset. Only the 1Hz PVT mode is now offered as a standard product.

The following sections describe the major differences between the ***ALLSTAR*** and the ***SUPERSTAR*** OEM boards.

2 FUNCTIONALITY

2.1 Protocol Selection & Non Volatile Memory

The Superstar offers to the NMEA user the possibility to set I/O operating mode in NMEA mode through discrete input levels. Disc_IP2 and Disc_IP_3 have the following functionality :

Disc_IP_3 (Protocol Select)	Disc_IP_2 (NVM Control)	Result
OPEN - HI	**OPEN – HI**	**Configuration stored in NVM or Default ROM Configuration if no valid NVM elements**
OPEN - HI	**GND**	**Protocol on Port #1: CMC Binary Baud Rate on Port #1 : 9600 Other elements : Default ROM Configuration**
GND	**OPEN – HI**	**Protocol on Port #1: NMEA Baud Rate on Port #1 : 4800 Other elements : Default ROM Configuration if no valid NVM elements**
GND	**GND**	**Protocol on Port #1: NMEA Baud Rate on Port #1 : 4800 Other elements : Default ROM Configuration**

Default Configuration if no valid NVM elements :

- Protocol on port #1: CMC Binary
- Baud Rate on port #1 : 9600
- Protocol on port #2 : RTCM-104
- Baud Rate on port #2 : 9600
- DGPS Correction Timeout : 45 seconds
- Msg List : Default ROM value
  CMC Binary : Navigation Status User Coordinates (#20) @ 1Hz
  NMEA : GGA @ 1Hz
- Time Align Mode : ON **(Note : OFF for the ALLSTAR)**

The data contained in the NVM is always used if the DISC_IP_2 is let disconnected or tied to a HI logic
If not, the default ROM configuration will be used and the following elements won't be used :

- Position
- Almanac
- Time
- UTC Correction and IONO Parameters
- TCXO Parameters

2.2 Memory Battery Back-Up

The Superstar can perform WARM_START without the need of an external supply source during POWER-OFF State.
An On-Board supercap allows the time-keeping circuit to be maintained for a period of 3 days over the temperature range (1 week typically).

3 MECHANICAL

3.1 CONNECTOR

3.1.1 I/O Connector (J1)

The connector shall be a 2mm straight header or right angle 2x10 position connector, PN from one suggested supplier is Samtec part number: TMM-110-03-T-D. A suggested mating connector could be Samtec 2mm Female connector part no. is TCSD-10-01-N. The cable could also be ordered as one piece using part no. TCSD-10-D-2.00-01-N (for a 2 inches flat cable with connector at each ends). Part no. TCSD-10-S-12.0-01-N has only one connector and is 12 inches long. You could also use a PCB mounted connector: SQT-110-01-L-D. With this mating connector, you shall use standoff of 0.340". It is recommended that you use this information as guidance only and you should get the latest connector specs from Samtec or other compatible manufacturers.

PIN #	Signal Name	Function
1	PREAMP	Power for active antenna (40 mA max)
2	VCC	Primary power (5V +10%/-5%)
3	VBATT	Back-up power for Real-Time clock device
4	RX_No_3/DISC_IO_3	Serial Intf RX #3 / ProgrammableDiscrete I/O pin Expansion pin for special application
5	MASTER_RESET	Reset Input pin (active LO)
6	DISC_IP_1	Reprogramming Control I/P pin
7	DISC_IP_3	Protocol Select Pin
8	DISC_IP_2	NVM Control pin
9	DISC_IO_1	ProgrammableDiscrete I/O pin Expansion pin for special application
10	GND	
11	TX_No_1	Serial Intf TX #1
12	RX_No_1	Serial Intf RX #1
13	GND	
14	TX_No_2	Serial Intf TX #2
15	RX_No_2	Serial Intf RX #2
16	GND	
17	DISC_IO_2	ProgrammableDiscrete I/O pin Expansion pin for special application
18	GND	
19	TIMEMARK	1 Pulse Per Second O/P
20	TX_No_3	Serial Intf TX #3 Expansion pin for special application

3.1.2 RF Connector (J2)

The standard RF connector is a straight SMT MCX jack connector. It is also possible to get a right angle MCX connector as an option.

The PN on the Superstar could be from Suhner: 648649 or from Johnson Comp.: 133-3711-208 or from Radiall: R113 424 020.

The mating straight connector could be Omni Spectra: 5831-5001-10 or Suhner: 11MCX-50-2-10C or Radiall: R113082.

The center conductor will supply active the antenna with the PREAMP signal from J1-1

3.1.3 Minimal Connections

The minimum number of connections required to have a working system is :

Signal name	**Pin #**
VCC	J1-2
Ground	J1-10, 13, 16 & 18
TX_No_1	J1-11
RX_No_1	J1-12

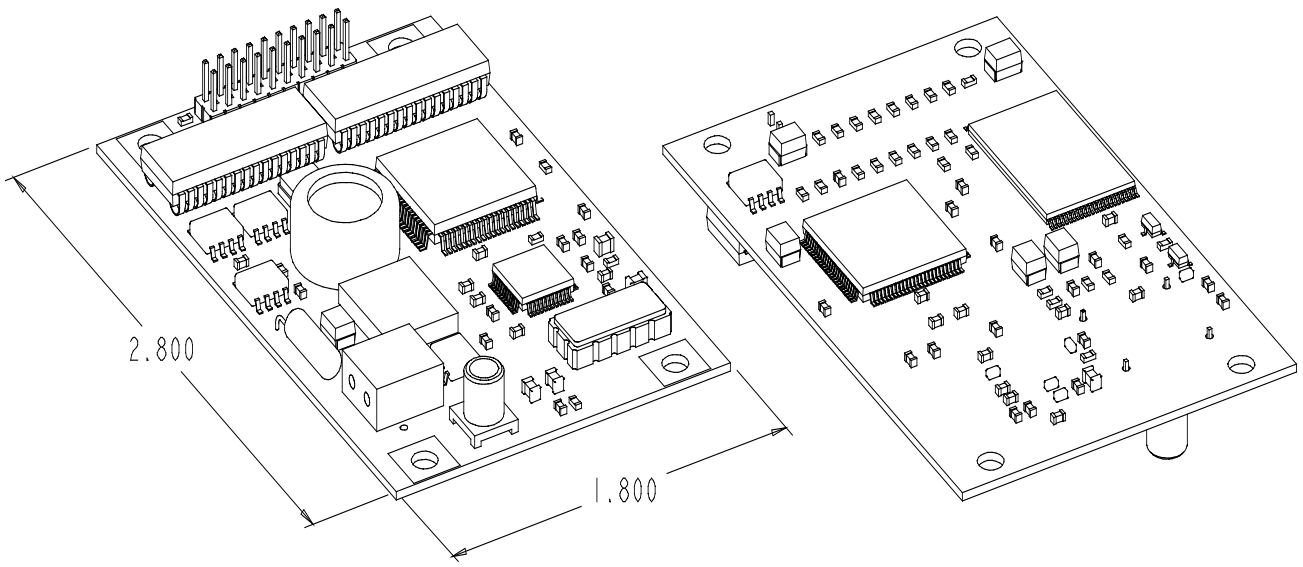
If **DGPS corrections** are required for the application, they could be transmitted to the SUPERSTAR through the Main Port or through the Auxiliary port

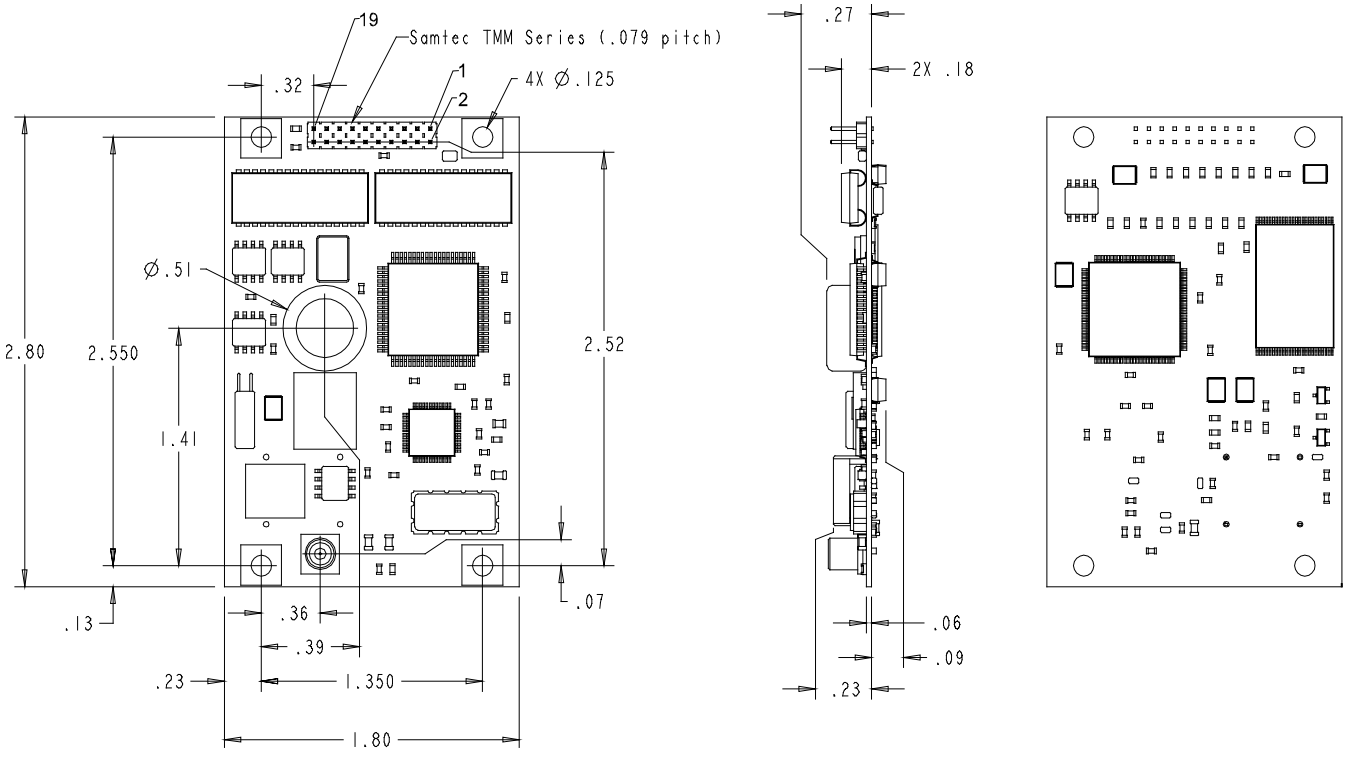
Signal name	**Pin #**
RX_No_2	J1-15

If an **active antenna** is used :

Signal name	**Pin #**
PREAMP	J1-1

3.2DIMENSIONS





4 ELECTRICAL SPECIFICATIONS

4.1 I/O Electrical Characteristics

All input pin shall have a valid state during reset and operating mode. No connection shall be required if the signal is not used in the application.

Signal Name	Type	Vil max Volt	Vih min Volt	Vol max Volt	Voh min Volt	Notes
MASTER_RESET	I	0.5	2.0			(1) (4)
DISC_IP_1, _2, _3 RX_No_1, _2	I	0.8	2.5			(3) (4) (6)
DISC_IO_1, _2	I/O	0.8	2.5	0.4	3.0	Io<=200uA (3),(5),(8)
TX_No_1, _2	O			0.4	3.0	Io<=200uA (4),(9)
RX_No_3/DISC_IO_3	I/O	0.8	2.0	0.4	3.7	Io<=200uA (3),(4),(8)
TIMEMARK TX_No_3	O			0.4	3.7	Io<=200uA (7),(8)

Note 1 : A LO pulse of 150ns will invoke a master reset to the Superstar (Max. 1usec rise & fall time)
Note 2 : Conditions : 5V +10%/-5% for all limits
Note 3 : Maximum input Voltage is 5.5V
Note 4 : All pins are in input mode during reset with pull-up resistor
Note 5 : All pins are in input mode during reset with pull-down resistor
Note 6 : DISC_IP_1 (Programming Ctrl Pin) is in input mode during reset with pull-down resistor
Note 7 : All pins are forced to an output logic level 0 during reset state
Note 8 : All output shall deliver a maximum current of 2mA

4.2 Power Requirements

4.2.1 PREAMP

Operating Voltage : 12Volts max
Current : 40mA max

4.2.2 VCC

VCC is the main and unique power source for normal operation

Max Operating Voltage : 5.5V
Operating Voltage : 5V [-5% +10%]

Ripple : 50mVp-p max

Power Consumption :	1.2W typ. 1.5W max
Standby Power Consumption (Master Reset Applied or VCC < 4.3Volts)	<0.25 W typ

4.2.3 VBATT

VBATT is an external back-up source for the Time Keeping Circuit. The Superstar has already a supercap device allowing WARM START for 1 week typically (@25 deg C) and 3 days over temperature range (-30 +75 deg C)

VBATT shall not be the same voltage level as the VCC. VBATT shall be 0.3Volt lower than VCC

Max Input Voltage :	5.0 V
Min Input Voltage :	2.0 V (required only to maintain time for a long time period)
Input Voltage during : Normal Operation	< VCC - 0.3V
Max Required Current :	0.5uA typical 1.5uA maximum (0 to 70 degree C)

5 SERIAL DATA INTERFACE

This section shows the differences in the CMC Binary protocol between the ALLSTAR and SUPERSTAR OEM boards. The NMEA protocol is identical for both products.

RECEIVER TO HOST CPU MESSAGES

A. MESSAGE SUMMARY

ID	DEFINITION	MESSAGE TYPE	RATE (SEC)	# BYTES
43	DGPS Configuration	UR		27
45	Hardware/Software identification request	UR	1	101
49	Receiver Status request	DR	1	12
51	Initiated BIT result	UR		40

LEGEND: CM : Command Message
DR : Data Request
PM : Protocol Message

B. MESSAGE CONTENT - RECEIVER TO HOST CPU

MESSAGE	BYTE	DESCRIPTION	UNIT	TYPE
43 DGPS Configuration	5	bit 0 : Enable (0=OFF, 1=On) bits 1-6: **Reserved** bit 7 : Port (0=Main, 1=Dedicated)	N/A	N/A
	6	Differential Coast Time	seconds	unsigned char
	7	Reserved	N/A	N/A
	8	Baud Rate (1=300, ... 32=9600, ... 64=19200)	300 bauds	N/A
	9..16	Messages requested for Retransmission (Bitmap: bit0 = 1, bit63 = 64) see message ID #83	N/A	N/A
	17..25	**Reserved**	N/A	N/A
45 Software Identification Information	5..18	Operational S/W Part number (XXX-XXXXXX-XXX)	N/A	char [14]
	19-32	First configuration Parameter block Part Number (XXX-XXXXXX-XXX)	N/A	char [14]
	33-36	First Configuration Parameter Block Checksum	N/A	unsigned long
	37..50	Boot S/W Part number (xxx-xxxxxx-xxx)	N/A	char [14]
	51	**Number of Config Block**	N/A	unsigned char
	52..54	**Variation block number 2**	N/A	unsigned char
	55..57	**Variation block number 3**	N/A	unsigned char
	58..60	**Variation block number 4**	N/A	unsigned char
	61..63	**Variation block number 5**	N/A	unsigned char
	64..66	**Variation block number 6**	N/A	unsigned char
	67..69	**Variation block number 7**	N/A	unsigned char
	70..72	**Variation block number 8**	N/A	unsigned char
	73..90	Reserved	N/A	N/A
	91..94	Boot Checksum	N/A	N/A
	95..98	Operational Checksum	N/A	N/A
	99	**Unit type** **bit 0-1: Unit type** **00b : Allstar** **10b: Superstar**	N/A	N/A

49 Receiver status data	5	bit **0: System Mode** **0 - Acquisition** **1 - Navigation** **bit 1..3: Reserved** **bit 4-5: Power Up Mode** **0: Normal Power Up** **1: PLL lock** **2: Watch Dog Reset** bit 6: Satellite tracking mode 0 - All SVs in view (based on current Almanac, position and time) 1 - Sky Search bit 7 : NVM Controller State 0 - Idle (no process in progress) 1 - Busy (Erase and/or Store data process in progress)	N/A	N/A
	6	bit 0 = 0: Tropo model enabled bit 1 = 0: MSL model enabled bits 2..3: Last Power-up Modes 0 - Cold Start (Invalid almanac, time or position) 1- Warm Start (Valid almanac, Time and Position) 2: Hot Start (Valid almanac, Time, Position and Ephemeris) bit 4: Reserved bits 5..7: Time Source 0 - Initialization required 1 - External 2 - SV without Nav 3 - SV with Nav	N/A	N/A
	7..8	Almanac Week of Collection	N/A	unsigned short
	9..10	Week number	N/A	unsigned short
	11..14	SV Deselect bitmap, byte 11: bit 0 = SV1 … byte 14: bit 7=SV32	N/A	N/A
	15..16	Channel Deselection bitmap, byte 15: bit 0 = Ch1 … byte 16: bit 7 - Ch12	N/A	N/A
	17..23	Reserved		
	24..25	Mask Angle	0.01 degree	**signed short**
	26	Discrete Inputs bit 0: DISC_IP1 bit 1: DISC_IP2		

49 (Cont'd)		bit 2: DISC_IP3 bit 3: DISC_IO1 bit 4: DISC_IO2 bit 5: DISC_IO3 bit 6-7: Reserved		
	27..28	TCXO Error Estimate	Hz	signed short
	29	TCXO Ageing	0.1 ppm	unsigned char
	30..33	Search Noise	dB	short float
	34	Nav Mode (see message #20 byte 71 for description)	N/A	
	35..44	Reserved	N/A	N/A
51 Initiated BIT Result	5	bit 0-7 : Copy of the Initiated BIT request message 0: Power Up BIT result 1: Initiated BIT result	N/A	N/A
	6	General Results (0=fail, 1=Pass) bit 0 : RAM bit 1 : Flash bit 2 : Eeprom bit 3 : Uart bit 4 : Real Time Clock bit 5 : Correlator & RF bit 6-7 : Reserved	N/A	N/A
	7..9	Reserved	N/A	N/A
	10	Memory Test Results (0=ok, 1=failure) bit 0 : Bad Boot S/W Checksum bit 1 : Bad Operational S/W Checksum bit 2-4: FLASH Error Code if different of 000 : Receiver can not be reprogrammed bit 5-7: Reserved	N/A	N/A
	11	EEPROM Status **bit 0: Link error** **bit 1: Memory location error**	N/A	N/A
	12	Primary Port (UART) results bit 0 : UART not ready or UART busy bit 1 : TX not full flag error bit 2 : No Data received during internal loop tests bit 3 : Framing or Parity error bit 4 : RX not full flag error **bit 5-7 : Reserved**	N/A	N/A
	13	Auxiliary Port (UART) results **(see byte 12 description)**	N/A	N/A
	14	RTC results **bit 0 :Serial link error** **bit 1: Date error** **bit 2: Time error** **bit 3: Data retention** bit 5-7 : Reserved	N/A	N/A

51 (Cont'd)	15	RF Test Results bit 0: MAG LO limit error bit 1: MAG HI limit error bit 2: SIGN LO limit error bit 3: SIGN HI limit error bit 4: I_Q Test error bit 5: PLL lock not valid bit 6-7: Reserved.	N/A	N/A
	16	Global Correlator test results #1 bit 0 : Channel 0 error in I&Q test … bit 7 : Channel 7 error in I&Q test	N/A	N/A
	17	Global Correlator test results #2 bit 0 : Channel 0 error in I&Q test … bit 7 : Channel 7 error in I&Q test	N/A	N/A
	18	Global Correlator test results #3 bit 0 : Channel 9 error in I&Q test bit 1 : Channel 10 error in I&Q test bit 2 : Channel 11 error in I&Q test bit 3 : Channel 12 error in I&Q test bit 4 : Channel 9 error in Measurement test bit 5 : Channel 10 error in Measurement test bit 6 : Channel 11 error in Measurement test bit 7 : Channel 12 error in Measurement test	N/A	N/A
	19-30	Reserved		
	31	**Serial Intf #3 (UART) results (see byte 12 description)**	N/A	N/A
	32-40	Reserved		