

TS-570D TS-570D

CIRCUIT DESCRIPTION

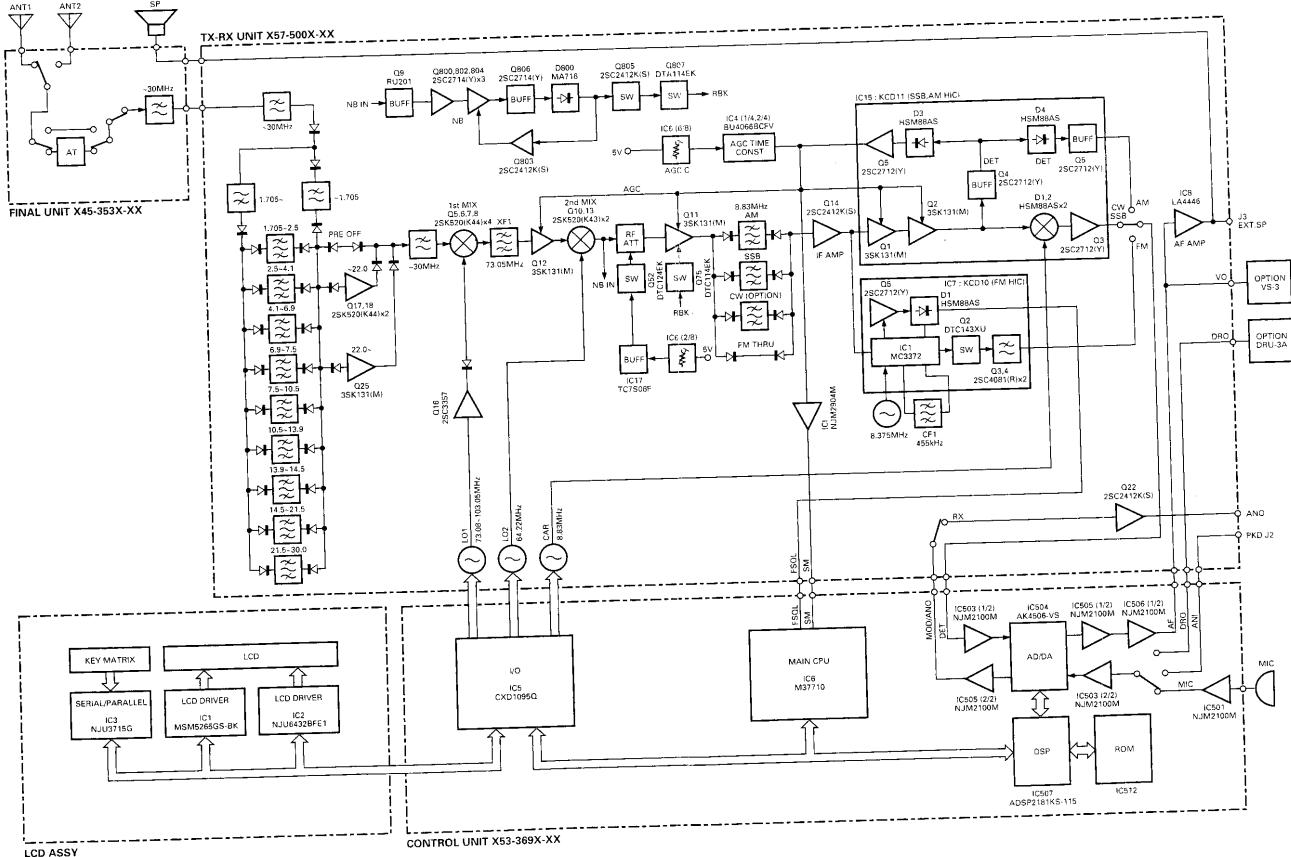


Fig. 5 Receiver section block diagram

TS-570D

CIRCUIT DESCRIPTION

TS-570D

CIRCUIT DESCRIPTION

Noise Blanker Circuits

The 8.83MHz IF signal generated by the second mixer is input to IF amplifier Q11: 3SK131, passes through buffer amplifier Q9: RU201, and amplified by noise amplifier Q800, Q802, and Q804: 2SC2714, passes through buffer amplifier Q806: 2SC2714, and noise-detected by D800: MA716. This signal switches Q805 and Q807 to control Q75 and Q15. It changes the source potential of the IF amplifier Q11 and blanks noise.

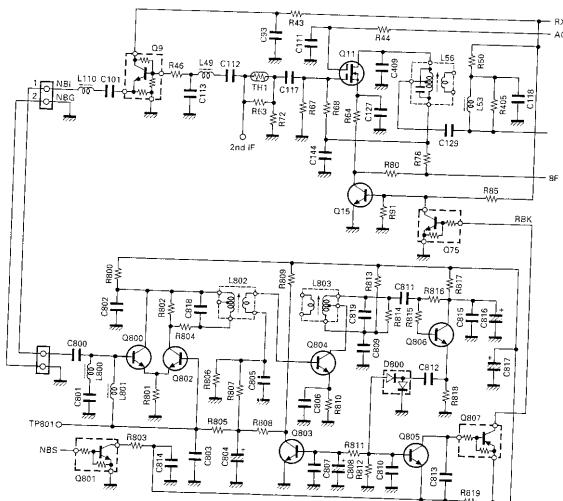


Fig. 7 Noise blanker circuits

AGC Circuit

The part of the IF signal amplified by IC15: KCD11 is envelope-detected for the AGC to control the AGC voltage. The AGC voltage is applied to the first and second amplifiers in IC15, the first IF amplifier Q12: 3SK131, and the second IF amplifier Q11: 3SK131. The time constant is changed by analog switch IC4: BU4066BCFV.

Signal-Strength Meter Circuit

In modes other than FM, the AGC voltage is inverted and amplified by operational amplifier IC1: NJM2904M. This output is used as the signal strength meter voltage. In FM mode, the level detection output from IC7: KCD10 is used. The signal strength meter voltage in each mode is switched by analog switch IC4: BU4066BCFV and output to the control unit.

Squelch Circuit

In FM mode, the noise detection voltage (FSQ1) output from IC7: KCD10 is sent to the control unit. In modes other than FM, the signal strength meter voltage is sent to the control unit. It is compared with the voltage proportional to the angle of the SQL VR to control squelch opening and closing. The microcomputer controls the delay time and hysteresis.

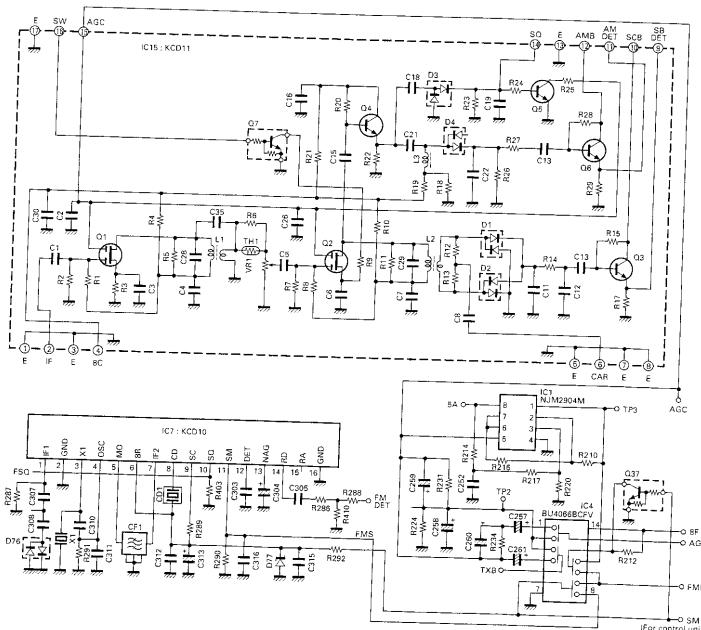


Fig. 8 AGC and S-meter circuits

TS-570D TS-570D CIRCUIT DESCRIPTION

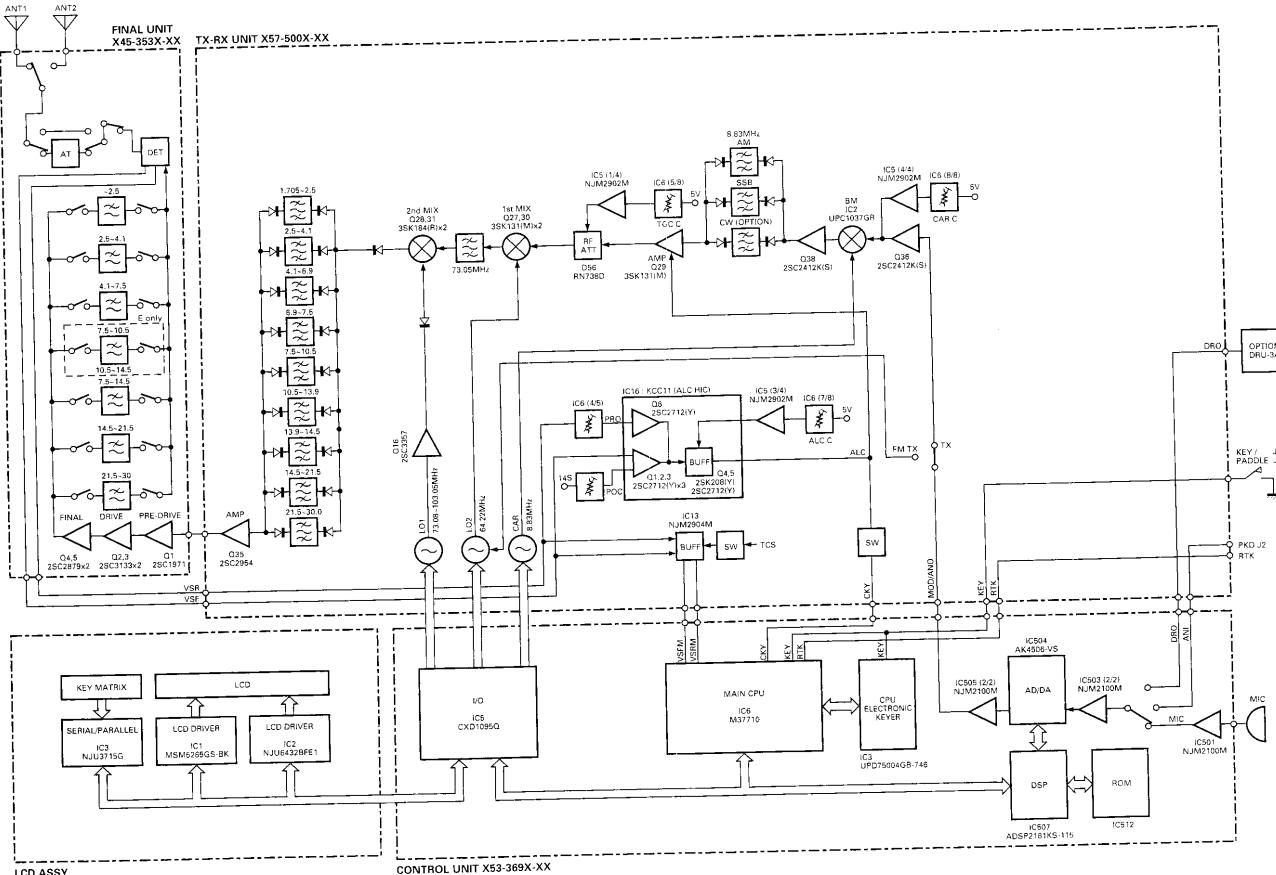


Fig. 9 Transmitter section block diagram

TS-570D CIRCUIT DESCRIPTION

■ Various Control Circuits by the Digital-to-Analog Converter

The circuits whose signal level was varied directly with a volume control or adjusted with a semi-fixed volume can be controlled by a microcomputer by using an eight-channel digital-to-analog converter.

CH No	Input pin No	Output pin No	Signal name	Control		Output destination
				1	2	
1	2	POC	Reference voltage, or power control			IC16 ALC circuit differential input
2	4	3	JFATT1: 21.5 to 30MHz IF gain reduction			IC17 AND gate
3	9	10	NC			
4	12	11	PRO: Reflected wave protection adjustment			IC16 protection input
5	13	14	TGC: Gain correction between bands and during power control			IC5 operational amplifier
6	16	15	AGC: AGC reference voltage adjustment			AGC circuit
7	21	22	ALC: ALC reference voltage adjustment			IC5 operational amplifier
8	24	23	CAR: CAR level adjustment			IC2 balanced modulator

Table 4 Digital-to-analog converter control

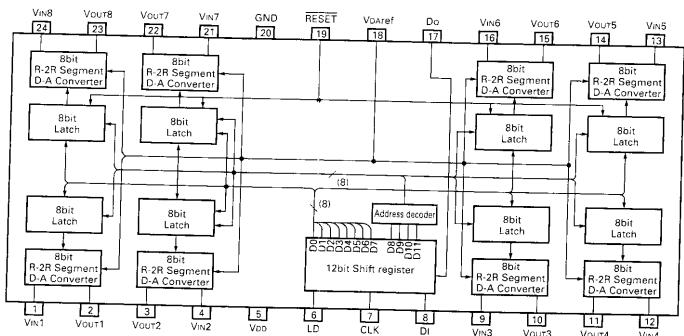


Fig. 13 M62363FP block diagram

TS-570D CIRCUIT DESCRIPTION

Digital Control

■ Overview

The TS-570D digital control circuit has multiple chips centered around the main CPU (IC6: M377010EBF), and consists of an electronic keyer microcomputer (IC3: UPD75004GB-746), an extended I/O (IC5: CXD1095Q) and DSP (IC507: ADSP2181KS-115). A block diagram of digital control is shown below.

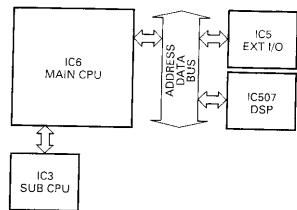


Fig. 14 Digital control section block diagram

CIRCUIT DESCRIPTION

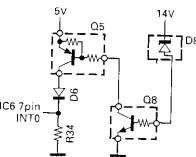


Fig. 15 Reset, backup circuits

■ Analog Signal Input

The main CPU incorporates a four-channel analog-to-digital (A/D) converter and a multiplexer (IC7 and IC8: TC4052BF) for entering 16-channel analog signals. Incoming analog signals are converted to digital values by the main CPU, which are used as digital data.

■ Display

The TS-570D uses a positive LCD and a semi-transparent display. The LCD is lighted with half a duty by the LCD driver.

■ PLL and DDS Data

The TS-570D has two PLLs and two DDSs in the PLL unit of the TX-RX unit. The main CPU sends data to the PLL ICs and DDS ICs according to the displayed frequency. The PLL ICs output unlock (UNL) signals. If one of the PLLs unlocks, the display shows that the PLL is unlocked.

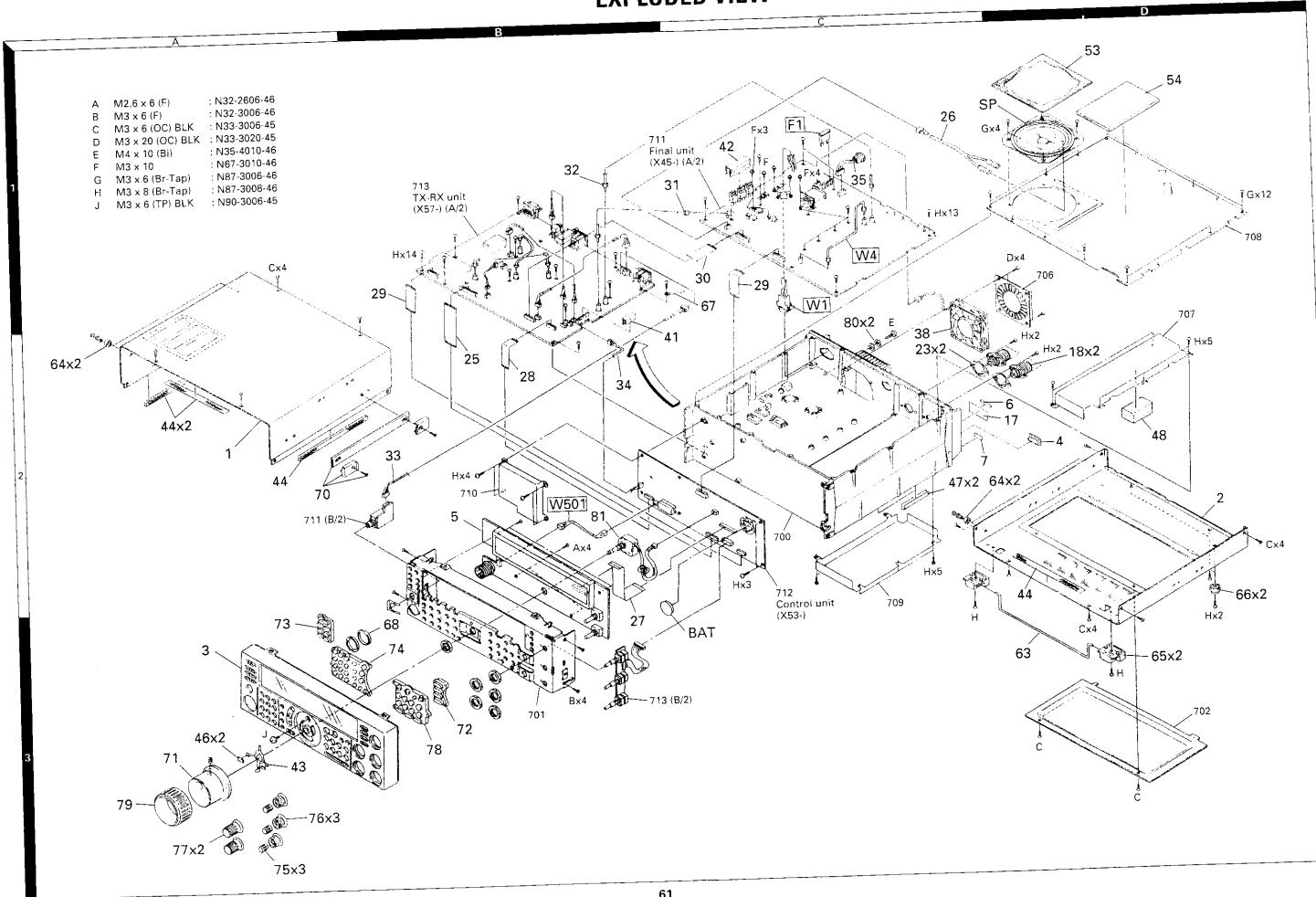
■ AT Control

The AT controlled by entering amplitude difference data (AMD) and phase difference data (PHD) to the main CPU, controlling the serial/parallel converter in the final unit, and changing the C capacity. The main CPU stores the serial/parallel converter data in each band, and whenever the frequency changes, the CPU outputs the data automatically to optimize antenna matching. The details of control of AMD terminal input and PMD terminal input are given below.

When AMD input is low, the CO count decreases. When AMD input is high, the CO count increases. When PMD input is low, the CI count decreases. When PMD input is high, the CI count increases.

TS-570D TS-570D
EXPLODED VIEW

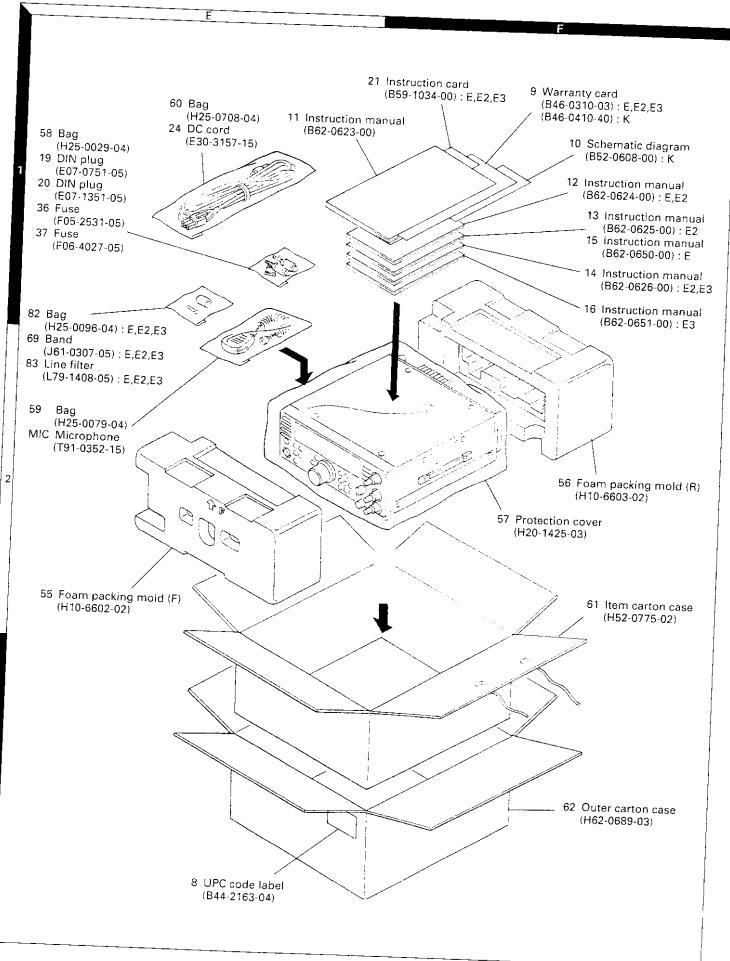
- | | | |
|---|-------------------|---------------|
| A | M 2.6 x 6 (F) | : N32-2606-46 |
| B | M 3 x 6 (F) | : N32-3006-46 |
| C | M 3 x 6 (OC) BLK | : N33-3006-45 |
| D | M 3 x 20 (OC) BLK | : N33-3020-45 |
| E | M 4 x 10 (BI) | : N35-4010-46 |
| F | M 3 x 10 | : N67-3010-46 |
| G | M 3 x 6 (Br-Tap) | : N87-3008-46 |
| H | M 3 x 8 (Br-Tap) | : N87-3008-46 |
| J | M 3 x 6 (TP) BLK | : N90-3006-45 |



Parts with the exploded numbers larger than 700 are not supplied.

TS-570D

PACKING



TS-570D

ADJUSTMENT

Required Test Equipment

1. DC Voltmeter (DC V.M.)

- 1) Input resistance : More than 1MΩ
- 2) Voltage range : 1.5 to 1000V AC/DC

Note : A high-precision multimeter may be used. However, accurate readings can not be obtained for high-impedance circuits.

2. DC Ammeter

- 1) Current range : 100mA, 1.5A, 15A, high-precision ammeter may be used.

3. RF VTVM (RF V.M.)

- 1) Input impedance : 1MΩ and less than 3pF, min.
- 2) Voltage range : 10mV to 300V
- 3) Frequency range : 10kHz to 500MHz

4. AF Voltmeter (AF V.M.)

- 1) Frequency range : 50Hz to 10kHz
- 2) Input resistance : 1MΩ or greater
- 3) Voltage range : 10mV to 30V

5. AF Generator (AG)

- 1) Frequency range : 200Hz to 2kHz
- 2) Output : 1mV or less to 1V, low distortion

6. AF Dummy Load (DM, SP)

- 1) Impedance : 8Ω
- 2) Dissipation : 3W or greater

7. Oscilloscope

Requires high sensitivity, and external synchronization capability (150MHz or greater).

8. Sweep Generator (Sweep G.)

- 1) Center frequency : 50kHz to 90MHz
- 2) Frequency deviation : Maximum ±35kHz
- 3) Output voltage : 100mV or greater

9. Standard Signal Generator (SSG)

- 1) Frequency range : 50kHz to 50MHz
- 2) Output : +13dBm/0.05μV to 7dBm/500mV
- 3) Output impedance : 50Ω
- 4) AM and FM modulation can be possible

Note : Generator must be frequency stable.

10. Frequency Counter (f. counter)

- 1) Minimum input voltage : 50mV
- 2) Frequency range : 150MHz or greater

11. Noise Generator (Noise G.)

Must generate ignition noise containing harmonics beyond 30MHz.

12. RF Dummy Load

- 1) Impedance : 150Ω and 50Ω
- 2) Dissipation : 150W or greater

13. Linear Detector

- 1) Frequency range : 30MHz

14. Power Meter

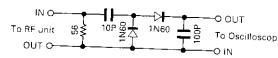
- 1) Impedance : 50Ω
- 2) Dissipation : 300W continuous or greater
- 3) Frequency limits : 60MHz or greater

15. Spectrum Analyzer

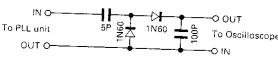
- 1) Frequency range : 100kHz to 110MHz or greater
- 2) Bandwidth : 1kHz to 3MHz

16. Detector

- 1) For adjustment of BPF



- 2) For adjustment of PLL/VCO BPF



17. Directional Coupler

18. Monitor Receiver R-1000 class

19. Microphone

MC-43S or MC-60S8

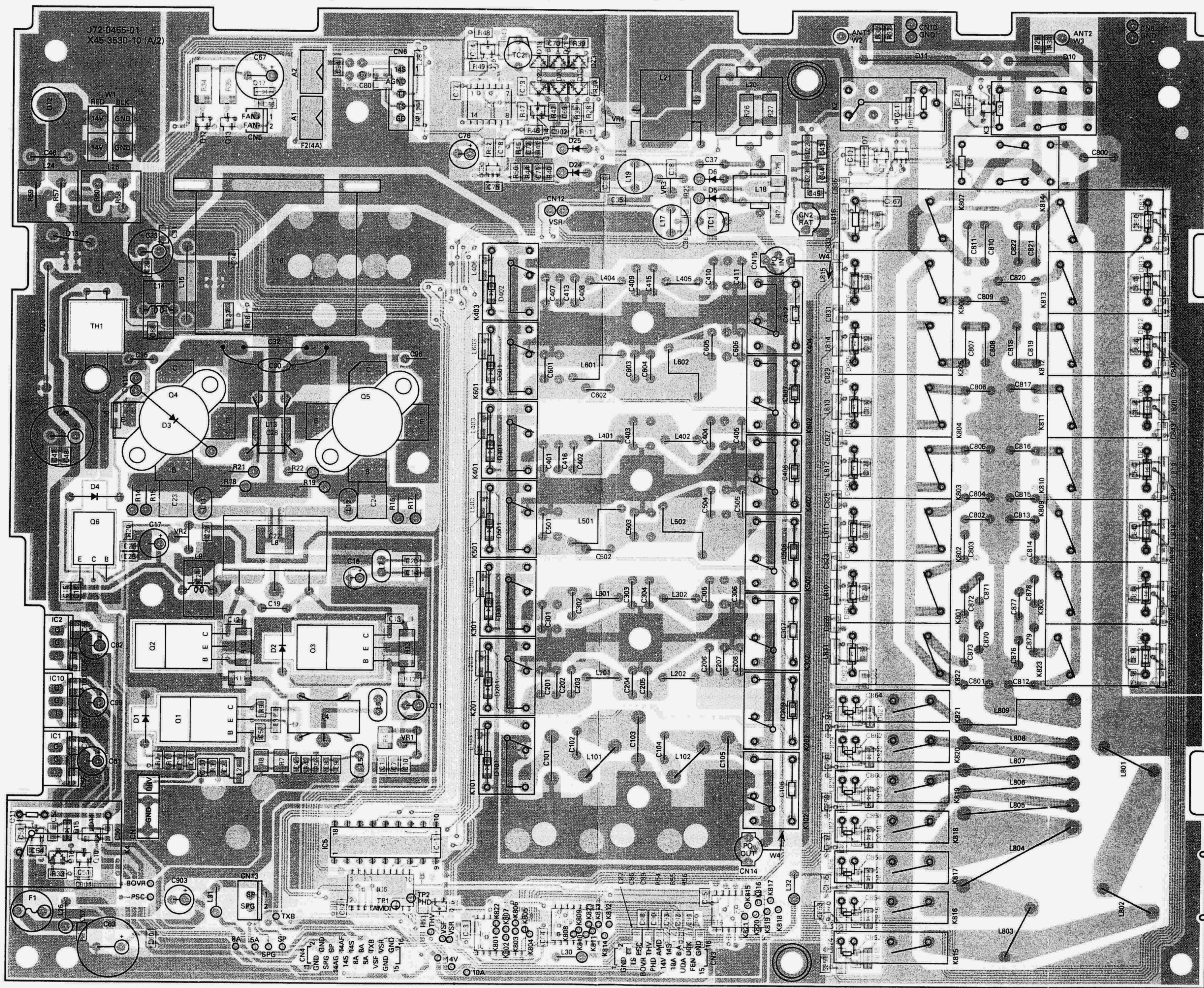
20. Tracking Generator

21. Distortion Meter

22. Double Signal Pad (50Ω)

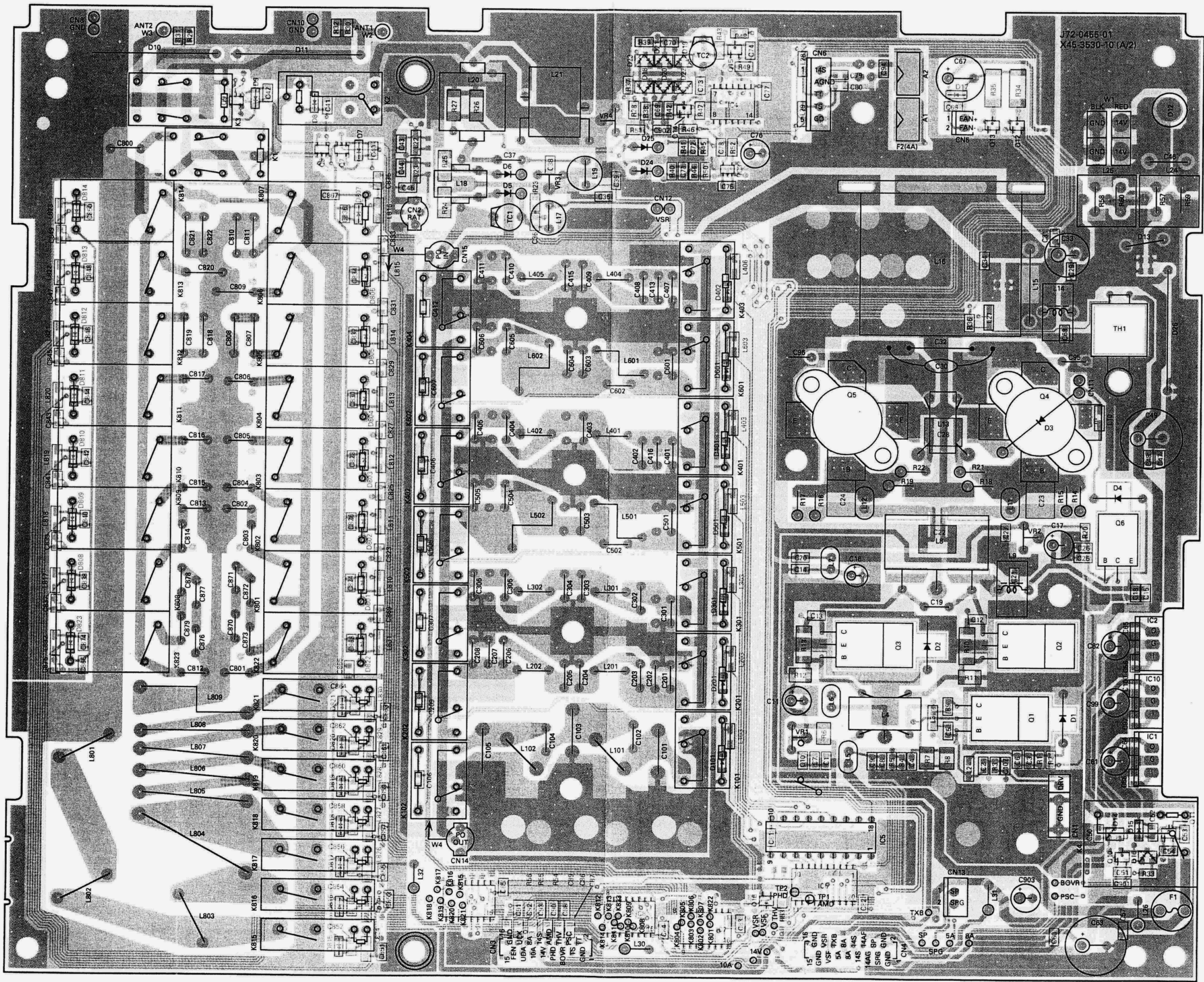
TS-570D PC BOARD VIEWS

FINAL UNIT (X45-353X-XX) (A/2) Component side view 0-10 : K,M2 2-71 : E,E2,E3



A horizontal sequence of seven black rectangles of varying widths arranged from left to right. Above each rectangle is a white capital letter: K, L, M, N, O, P, Q, R, S, T. The rectangles are positioned such that their centers align vertically along a horizontal axis.

FINAL UNIT (X45-353X-XX) (A/2) Foil side view 0-10 : K,M2 2-71 : E,E2,E3

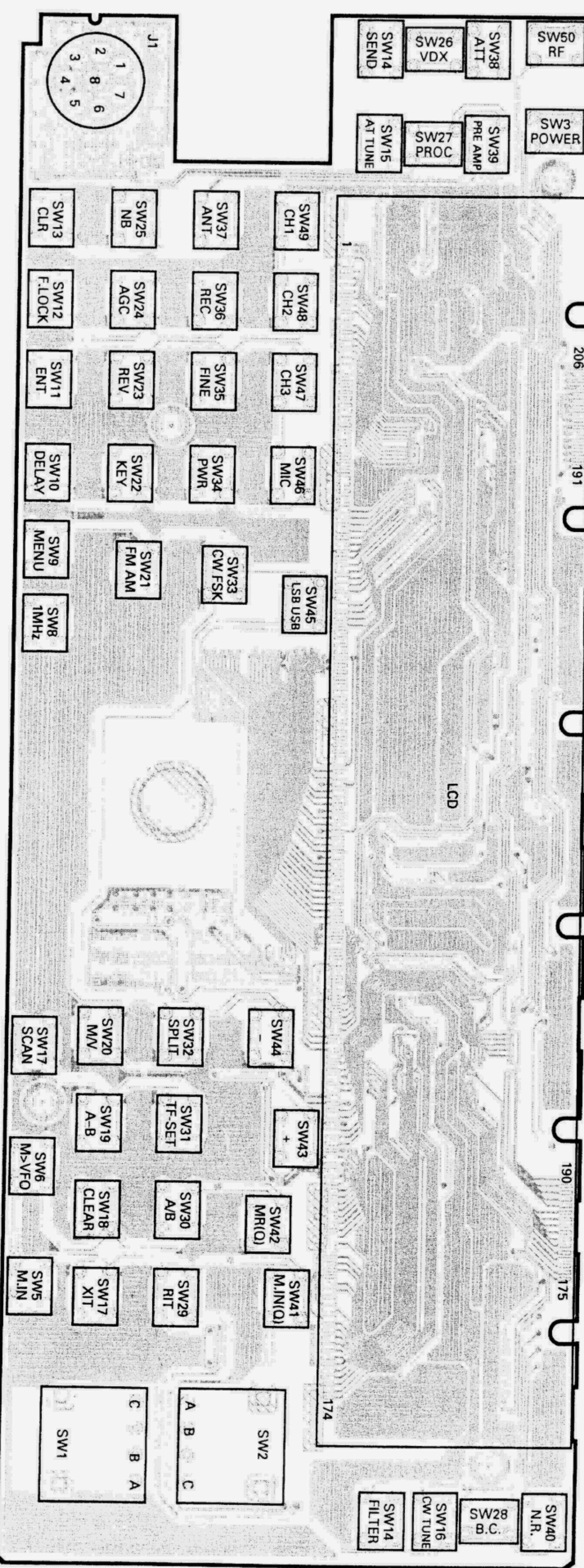


- Component side
- Foil side

A B C D E F G H I J

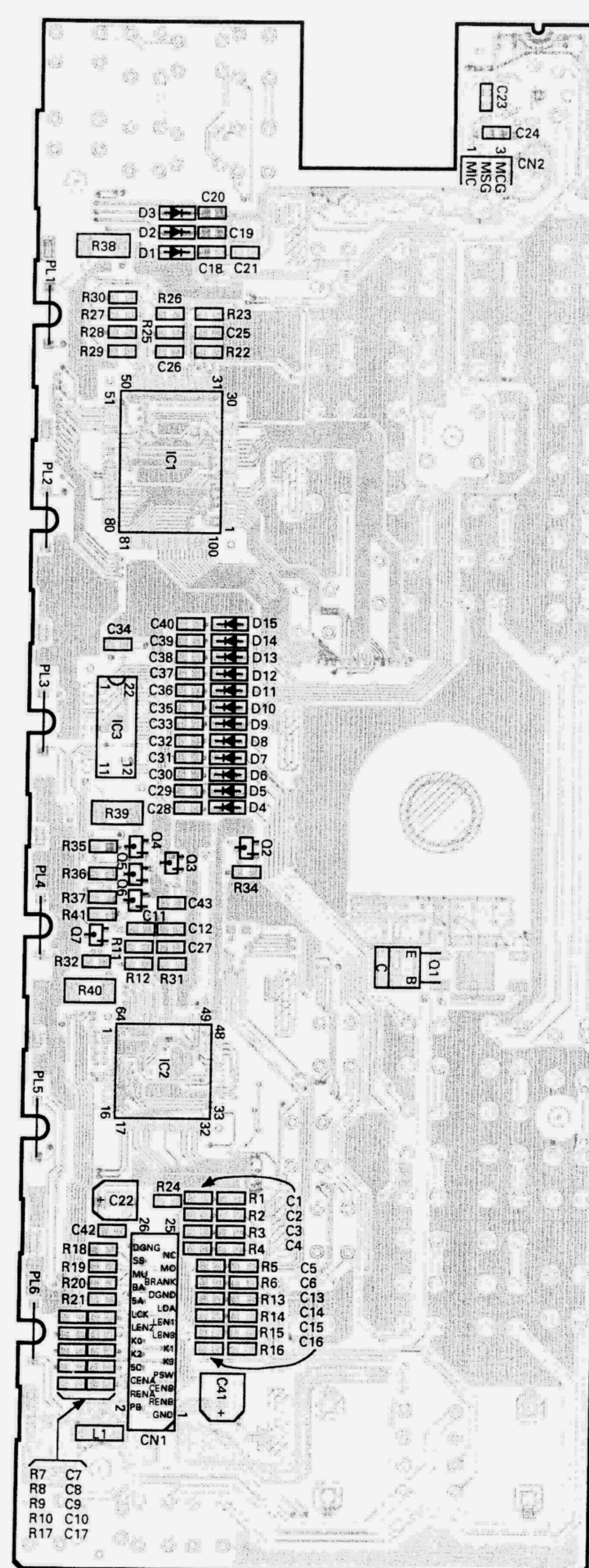
LCD ASSY (B38-0765-05)

Component side view

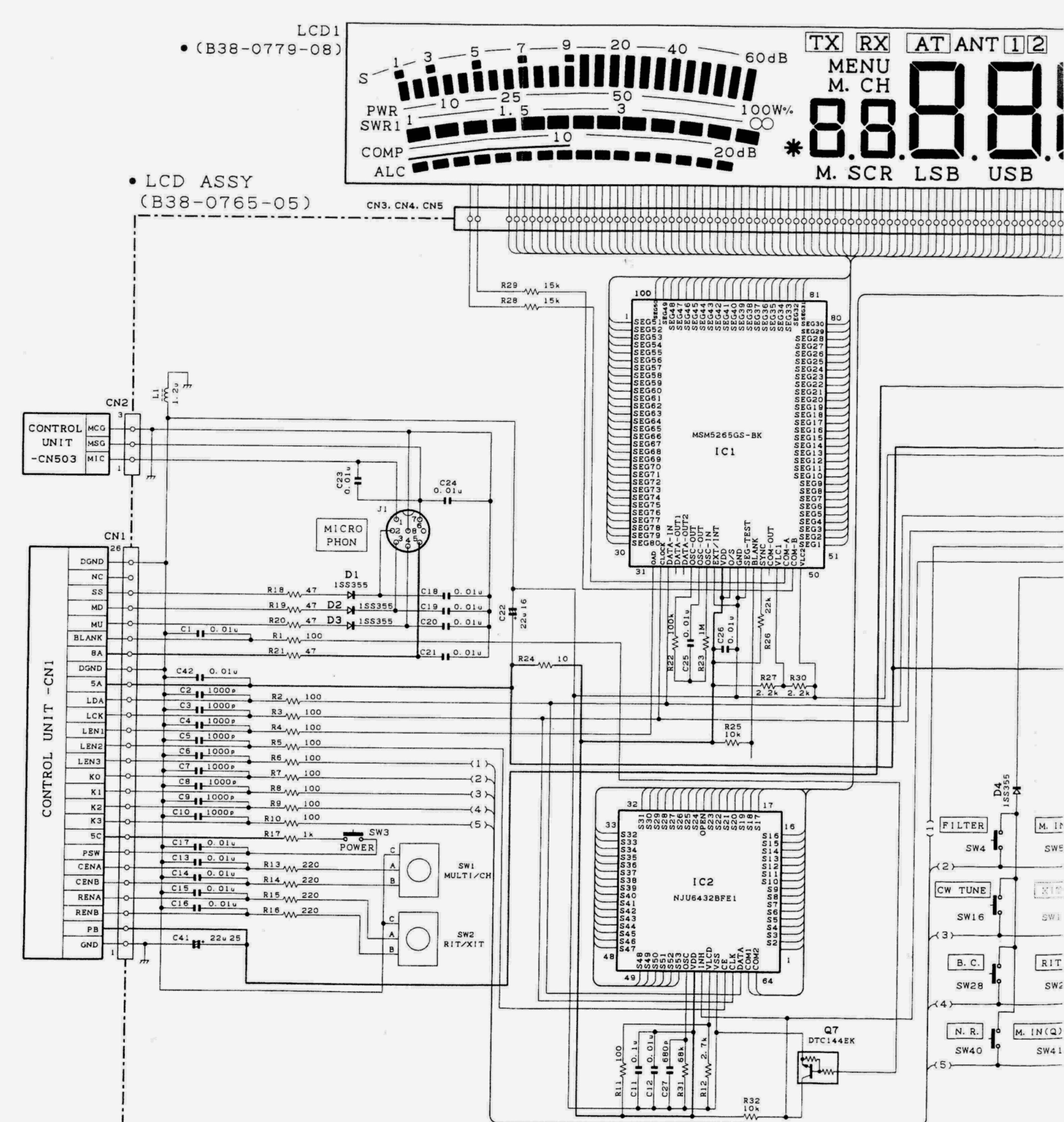


LCD ASSY (B38-0765-05)

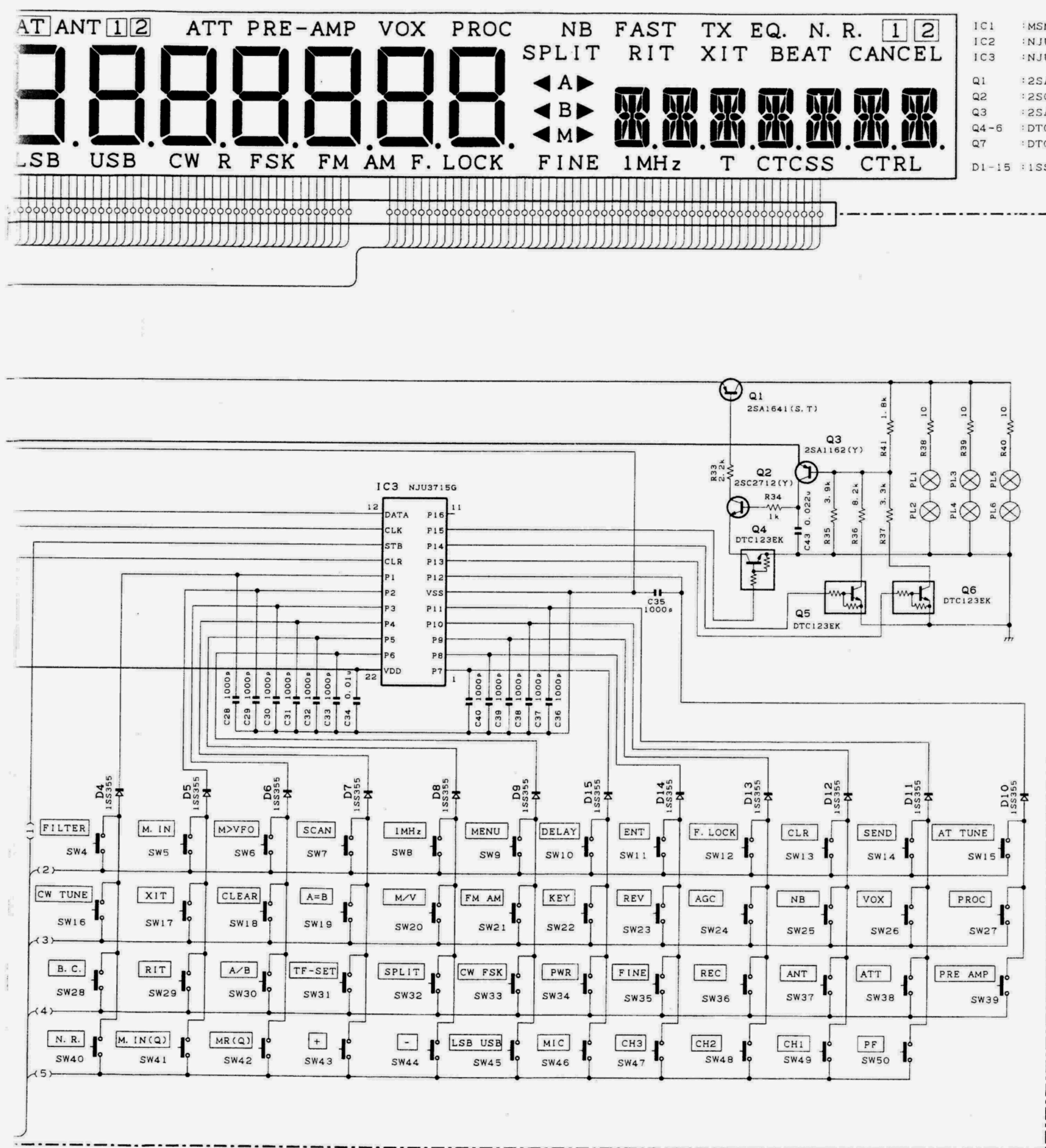
Foil side view



LCD ASSY (B38-0765-05)



PC BOARD VIEWS / CIRCUIT DIAGRAM TS-570D

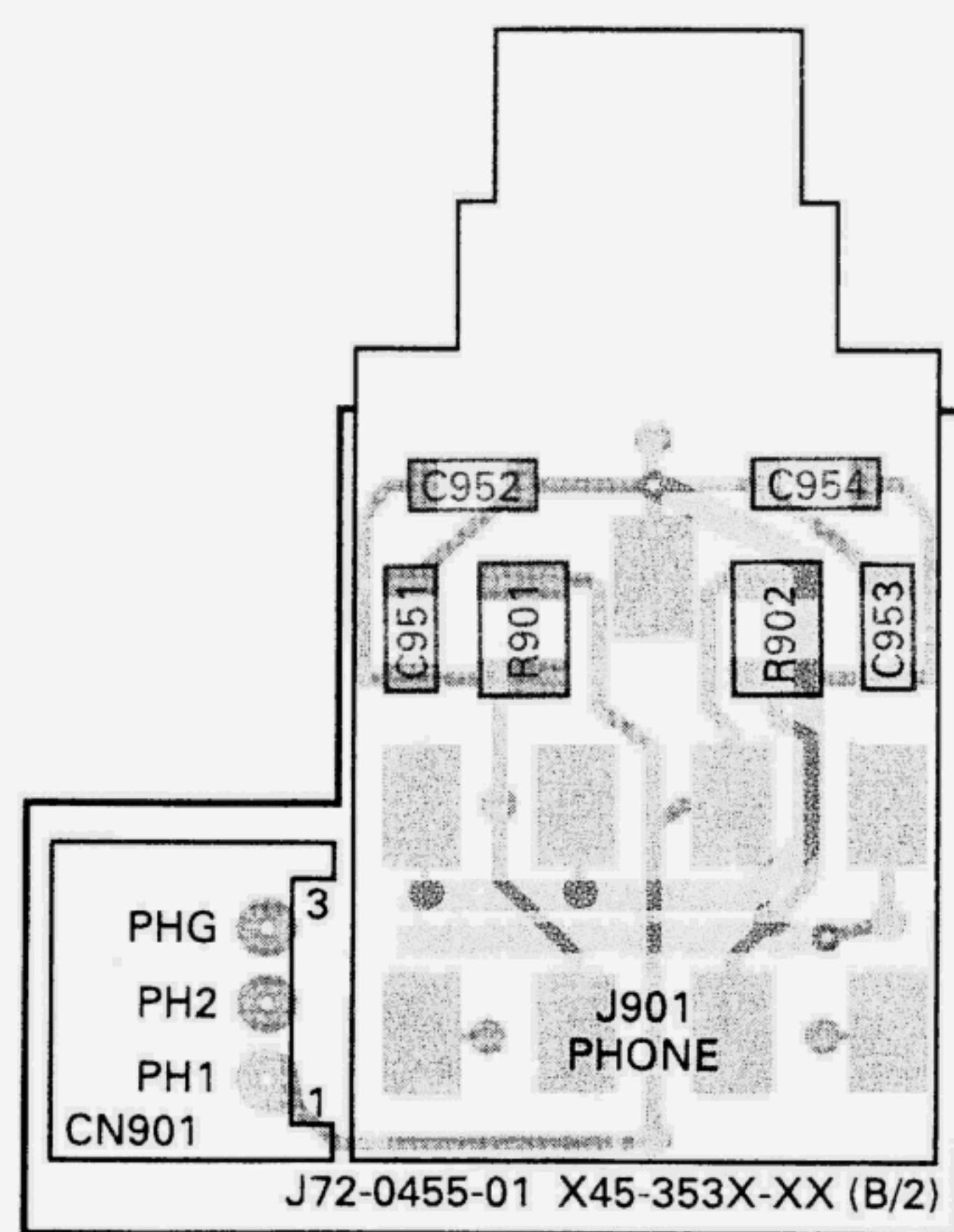


FINAL UNIT (X45-353X-XX) (B/2) : PHONE

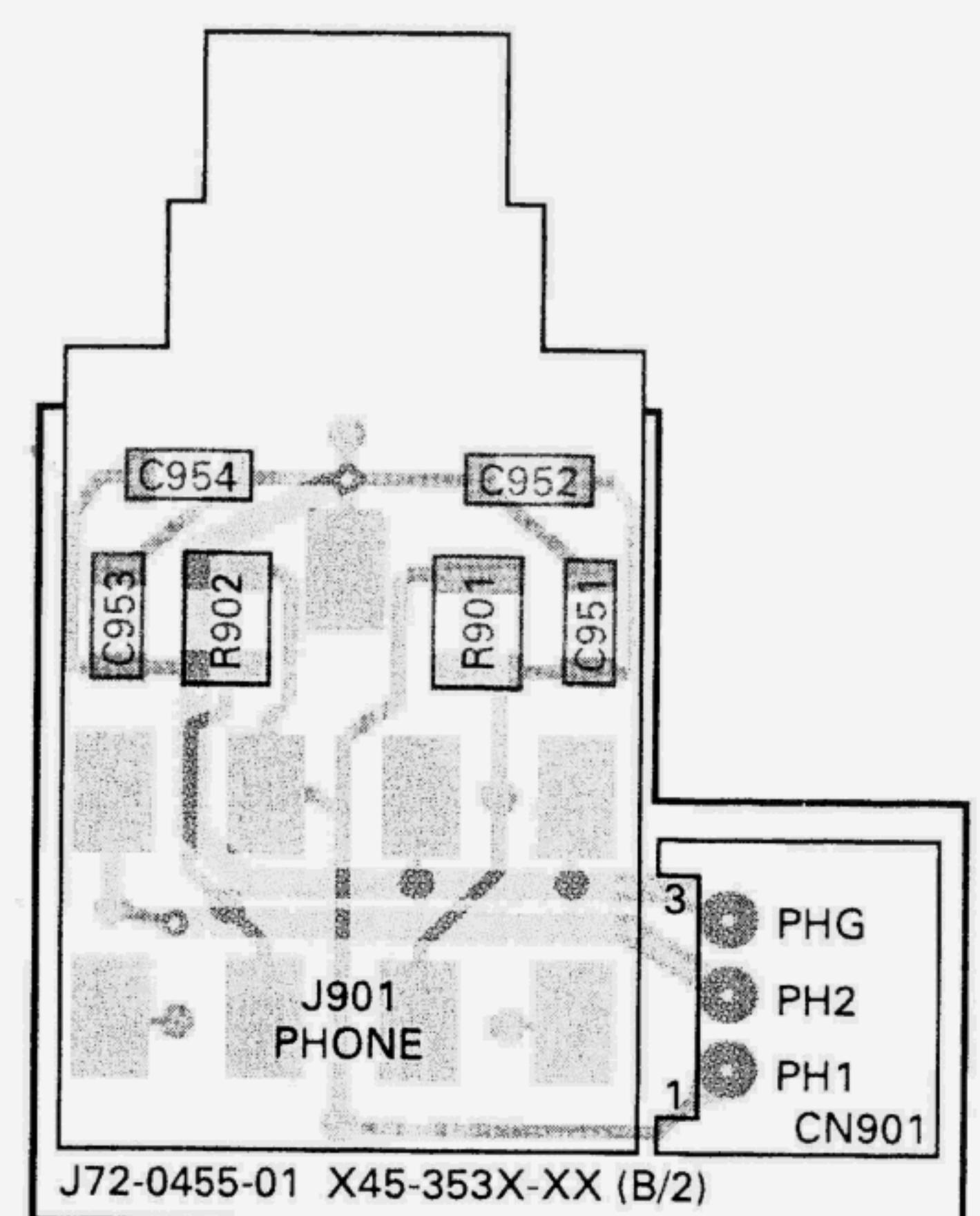
0-10 : K,M2 2-71 : E,E2,E3

Component side view

Foil side view



J72-0455-01 X45-353X-XX (B/2)



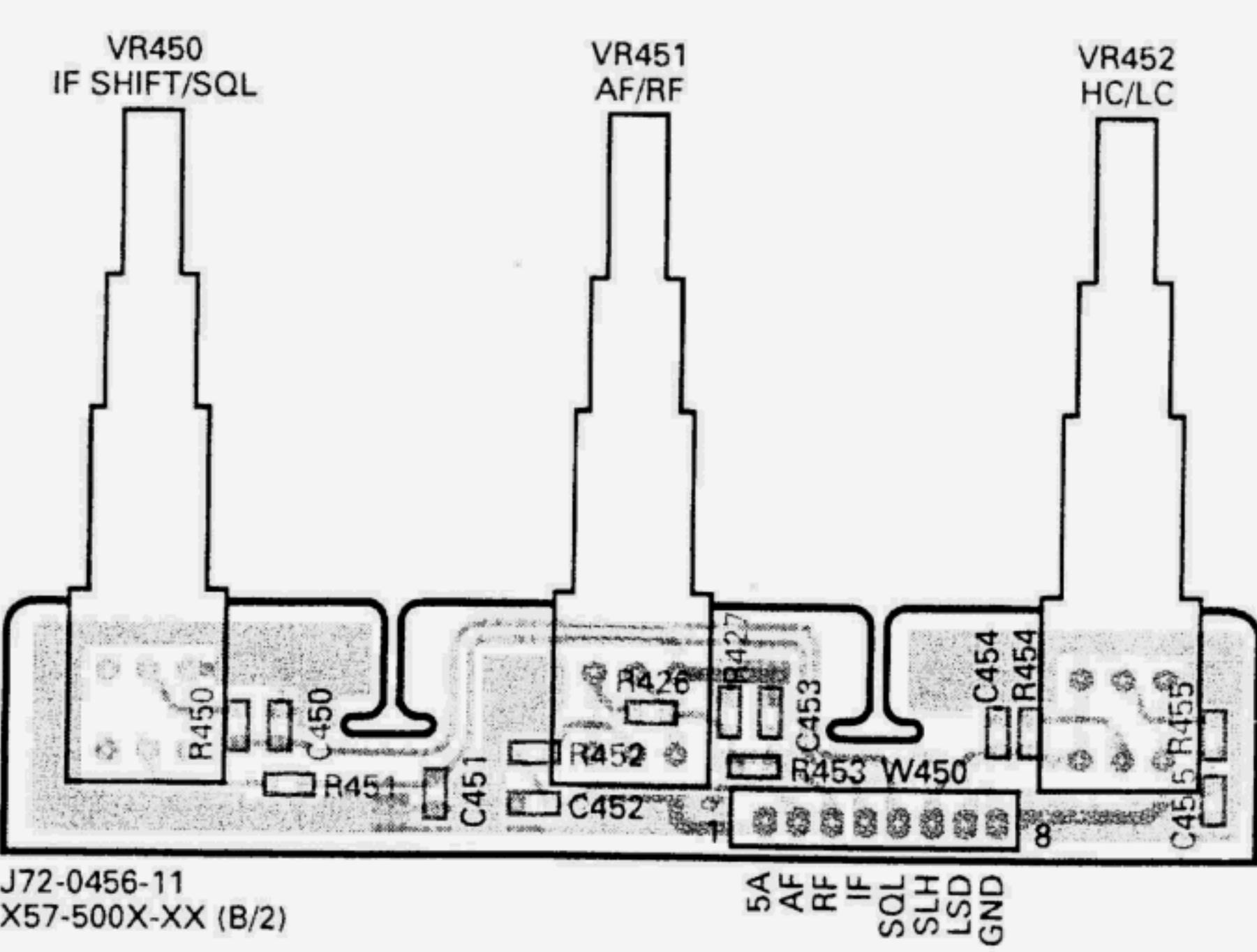
J72-0455-01 X45-353X-XX (B/2)

TX-RX UNIT (X57-500X-XX) (B/2) : VOLUME

0-10 : K,M2 2-71 : E,E2,E3

Component side view

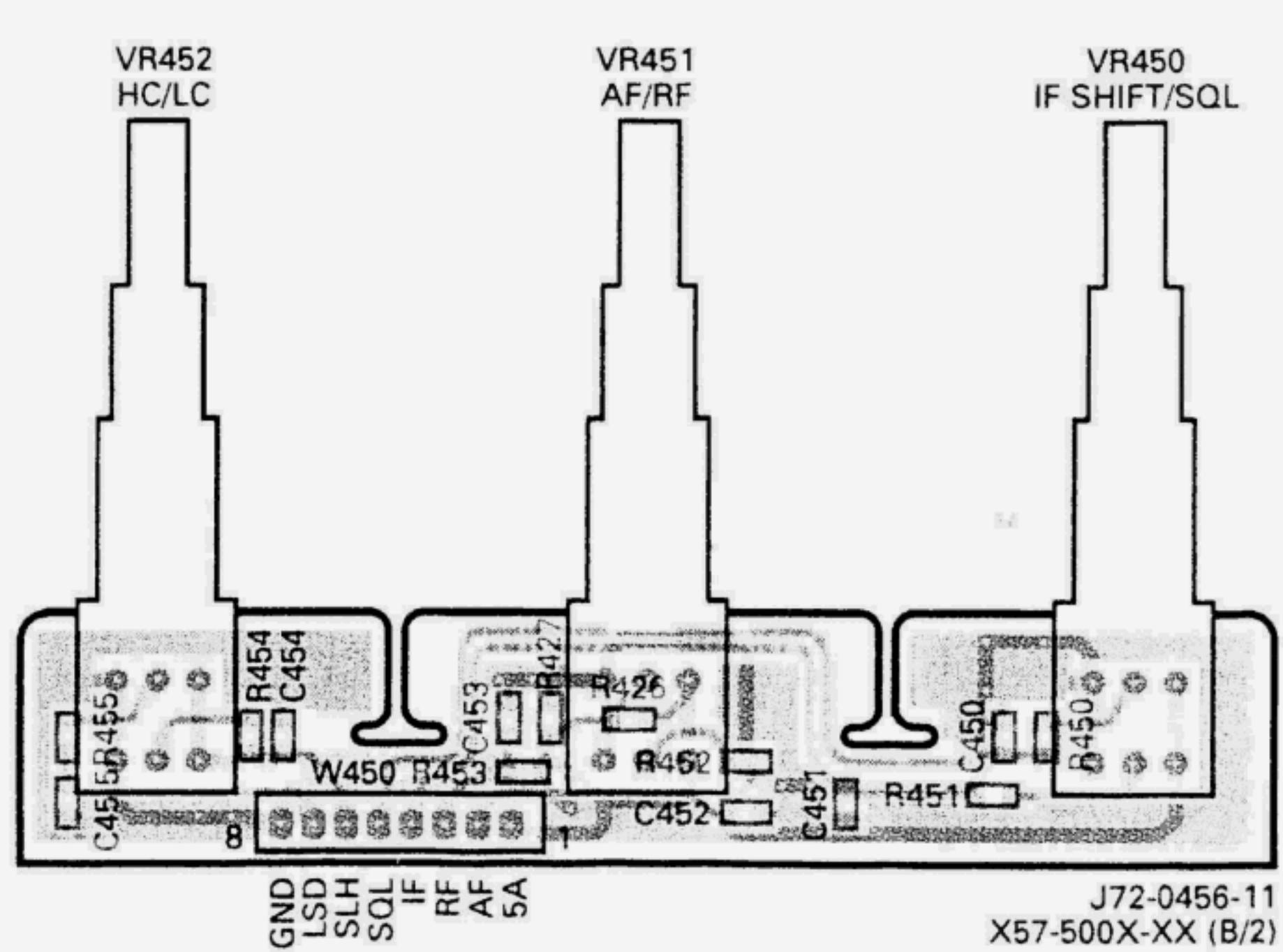
Foil side view



J72-0456-11
X57-500X-XX (B/2)

Component side

Foil side



J72-0456-11
X57-500X-XX (B/2)

A

B

C

D

E

F

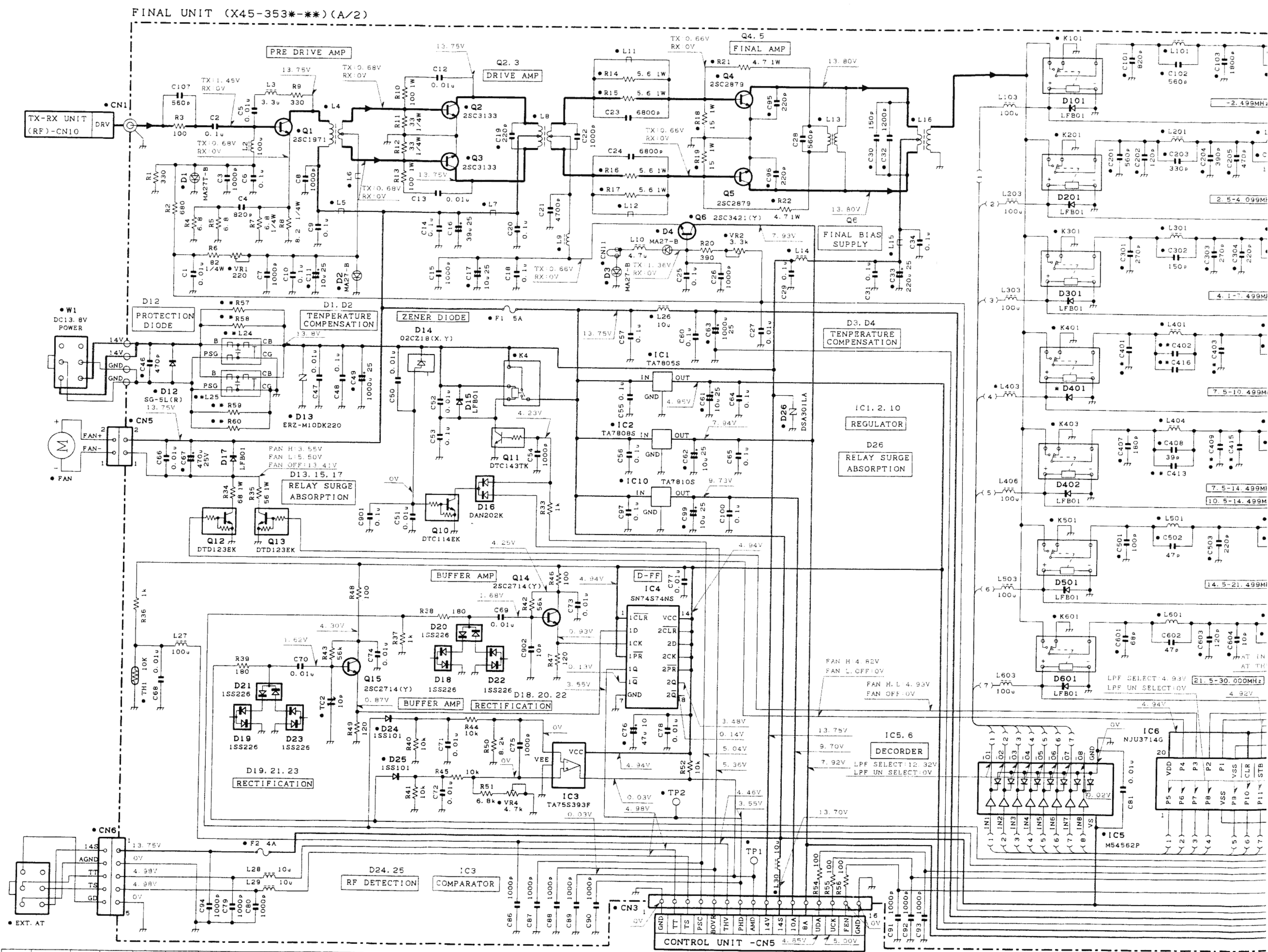
G

H

I

J

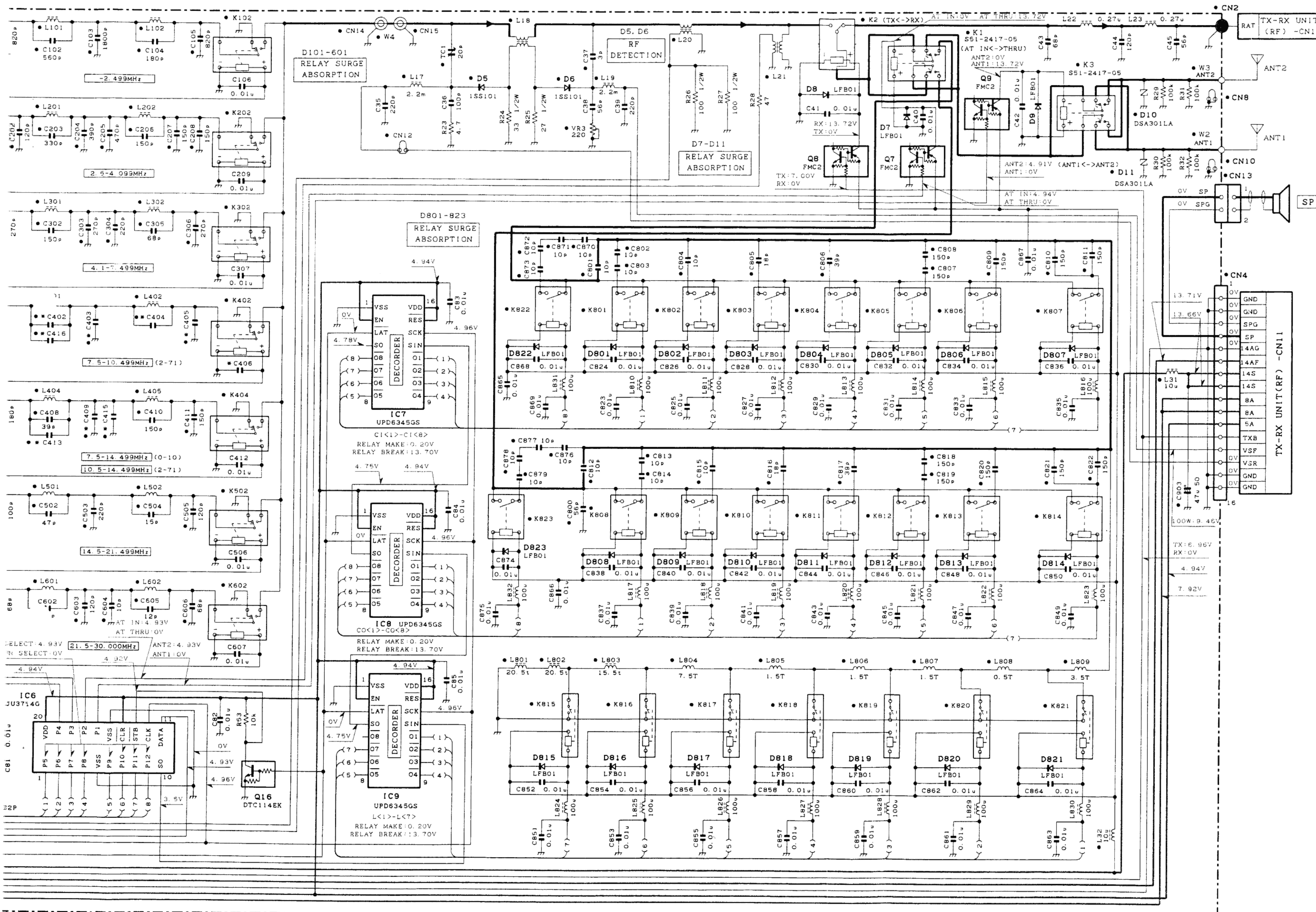
FINAL UNIT (X45-353X-XX) 0-10 : K,M2 2-71 : E,E2,E3



	C401	C402	C403	C404	C405	C406	C409	C413	C415	C416	D401	K401	K402	L24	L25	L401	L402	L403	R57	R58	R59	R60	T401.402		
0-10	K. M2	-	-	-	-	180 μ	5 μ	120 μ	-	-	-	-	-	-	-	-	-	-	-	-	-	-	D1 : MA27T-		
2-71	E. E2, E3	180 μ	47 μ	270 μ	150 μ	150 μ	0.01u	330 μ	-	-	5 μ	LFB01	S54-1420-05	S54-1420-05	L79-0558-05	L79-0558-05	L79-1221-05	L79-1221-05	L40-1015-48	R52-2569-05	R52-2569-05	R92-2569-05	R92-2569-05	R92-0108-05	D2-4 : MA27-B

D1 : MA27T-
D2-4 : MA27-B
D5. 6. 24. 25 : ISS101

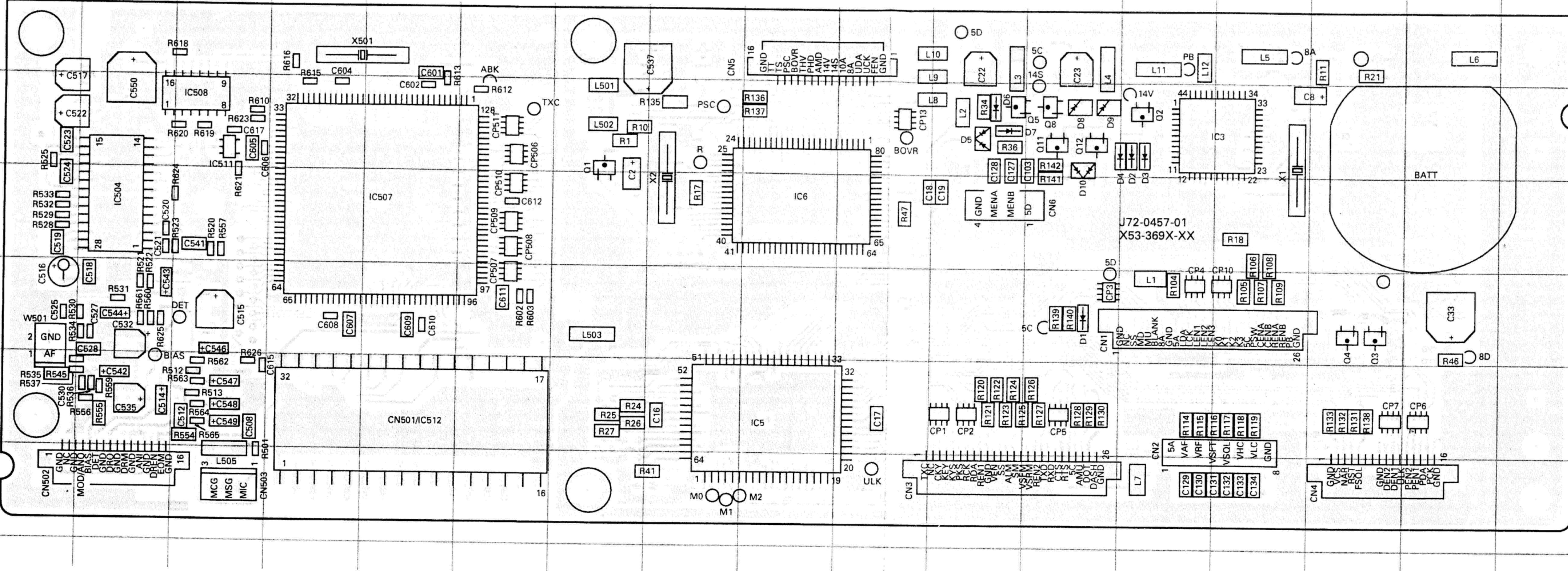
CIRCUIT DIAGRAM TS-570D



D1	:MA27T-B	D7-9, 15, 17, 101, 201, 301, 401.	D12 :SG-5L(R)	D16 :DAN202K	Q4, 5 :2SC2879	Q11 :DTC143TK	IC1 :TA7805S	IC4 :SN74S74NS	IC7-9 :UPD6345GS
D2-4	:MA27T-B	402, 501, 601, 801-823	:LFBO1	D13 :ERZ-M10DK220	D18, 19, 20-23 :ISS226	Q6 :2SC3421(Y)	Q12, 13 :DTD123EK	IC2 :TA7808S	IC5 :M54562P
D5, 6, 24, 25	:ISS101	D10, 11, 26	:DSA301LA	D14 :02CZ18(X, Y)	Q1 :2SC1971	Q7-9 :FMC2	Q14, 15 :2SC2714(Y)	IC3 :TA785S393F	IC6 :NJU3714G

TS-570D PC BOARD VIEWS

CONTROL UNIT (X53-369X-XX) Component side view 0-10 : K 0-21 : M2 2-71 : E 2-72 : E2 2-73 : E3



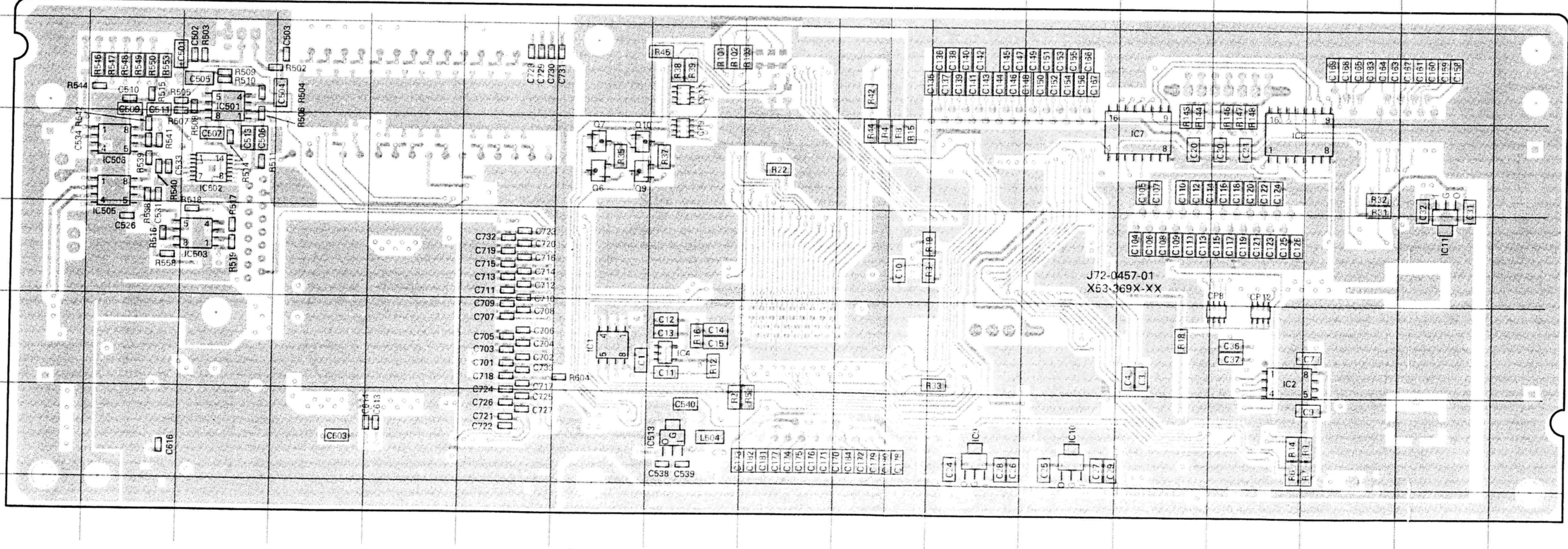
Ref. No.	Address	Ref. No.	Address
IC3	3M	Q8	3L
IC5	6I	Q11	3L
IC6	4I	Q12	3L
IC504	4B	D1	5L
IC507	4E	D2	3M
IC508	3C	D3	3M
IC511	3C	D4	3M
IC512	6E	D5	3K
Q1	3G	D6	3K
Q2	3M	D7	3K
Q3	5O	D8	3L
Q4	5O	D9	3L
Q5	3K	D10	3L

Component side

Pattern 1	
Pattern 2	
Pattern 3	
Pattern 4	

Foil side

CONTROL UNIT (X53-369X-XX) Foil side view 0-10 : K 0-21 : M2 2-71 : E 2-72 : E2 2-73 : E3



Ref. No.	Address	Ref. No.	Address
IC1	12G	IC502	10C
IC2	12N	IC503	11C
IC4	12H	IC505	10B
IC7	10M	IC506	10B
IC8	10N	IC513	13H
IC9	13K	D6	10G
IC10	13L	D7	10G
IC11	11P	D9	10G
IC501	9C	D10	10G

Component side

- Pattern 1
- Pattern 2
- Pattern 3
- Pattern 4

Foil side

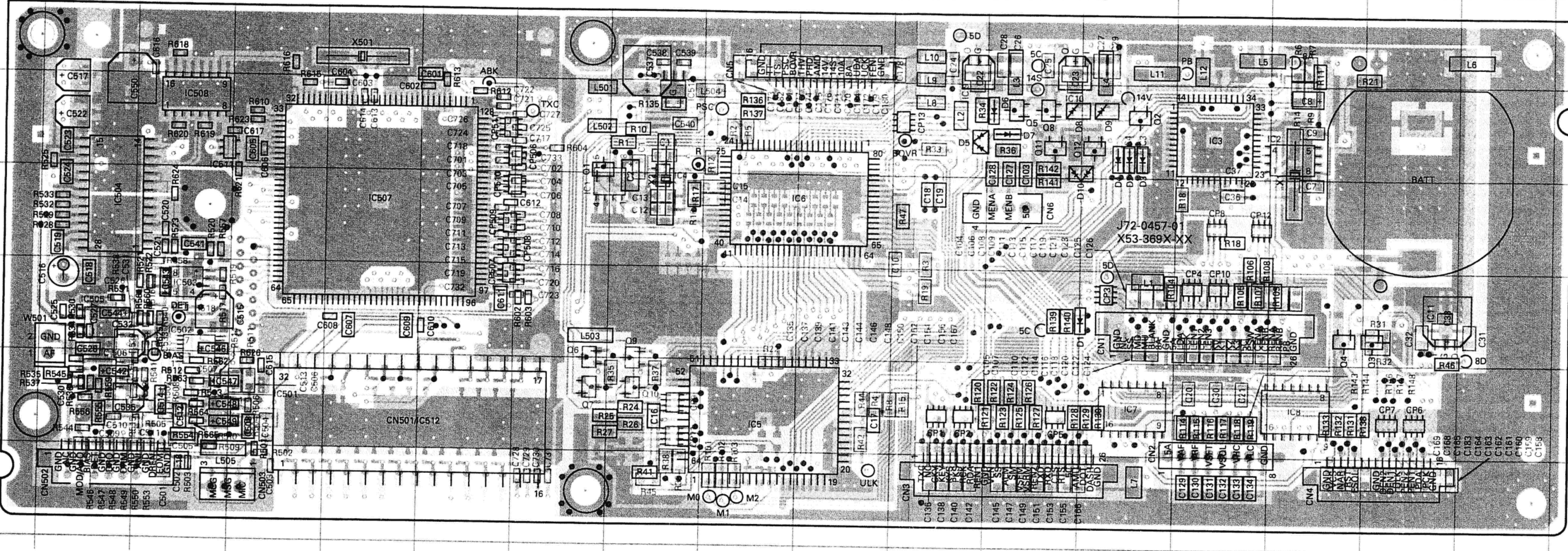
DTA
DTA
DTA
DTC
DTC
DTC
DTC
DTC
DTC
DTD

TAZ

NJU:

T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	AM
---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----

CONTROL UNIT (X53-369X-XX) Component side view + Foil side 0-10 : K 0-21 : M2 2-71 : E 2-72 : E2 2-73 : E3



Ref. No.	Address	Ref. No.	Address
IC1	4Z	Q1	3Z
IC2	3AH	Q2	3AF
IC3	3AG	Q3	5AI
IC4	3AA	Q4	5AH
IC5	6AB	Q5	3AE
IC6	4AB	Q6	5Z
IC7	6AF	Q7	6Z
IC8	6AI	Q8	3AE
IC9	2AD	Q9	5AA
IC10	2AE	Q10	10AA
IC11	5AI	Q11	3AE
IC501	6V	Q12	3AF
IC502	5V	D1	5AE
IC503	5V	D2	3AF
IC504	4U	D3	3AF
IC505	5U	D4	3AF
IC506	6U	D5	3AD
IC507	4X	D6	3AE
IC508	3V	D7	3AE
IC511	3V	D8	3AE
IC512	6X	D9	3AF
IC513	3AA	D10	4AE

Component side

- Pattern 1
- Pattern 2
- Pattern 3
- Pattern 4

Foil side

● Connect 1 and 4

Address
10C
11C
10B
10B
13H
10G
10G
10G
10G

2SB1188
2SC2954
2SC3357
2SD1624

2SC3421

2SA1641

2SC3133

2SC1971

2SC2879

2SK1875
2SK520

TA7805S
TA7808S
TA7810S

NJM78L05UA
NJM78L06UA
NJM78L08UA

FMA5
FMC2
FMG3A

3SK131
3SK184
RU201

TA75S393F

BU4S66
PST9121NR
TC7S04F
TC7S08F

AT24C64N10S127
CAT35C102KI
NJM2100M
NJM2904M
UPC1037GR
UPC1686G

LA4446

SN76514N

BU4066BCFV
NJM2902M
SN74S74NS

ADM232LAR
TC4052BF
TC9174F

TC74HC4040AF

BU2090FS
MB86001PF
UPD6345GS

M54562P

NJU3714G

NJU3715G

M62363FP

AK4506-VS
NJU3718G

F71022
UPD75004GB-746

CXD1095Q

NJU6432BFE1

M37710EFBJQF *

MSM5265GS-BK

ADSP2181KS-115

27C01012DJPHB

A

B

C

D


E

F


G

H

J

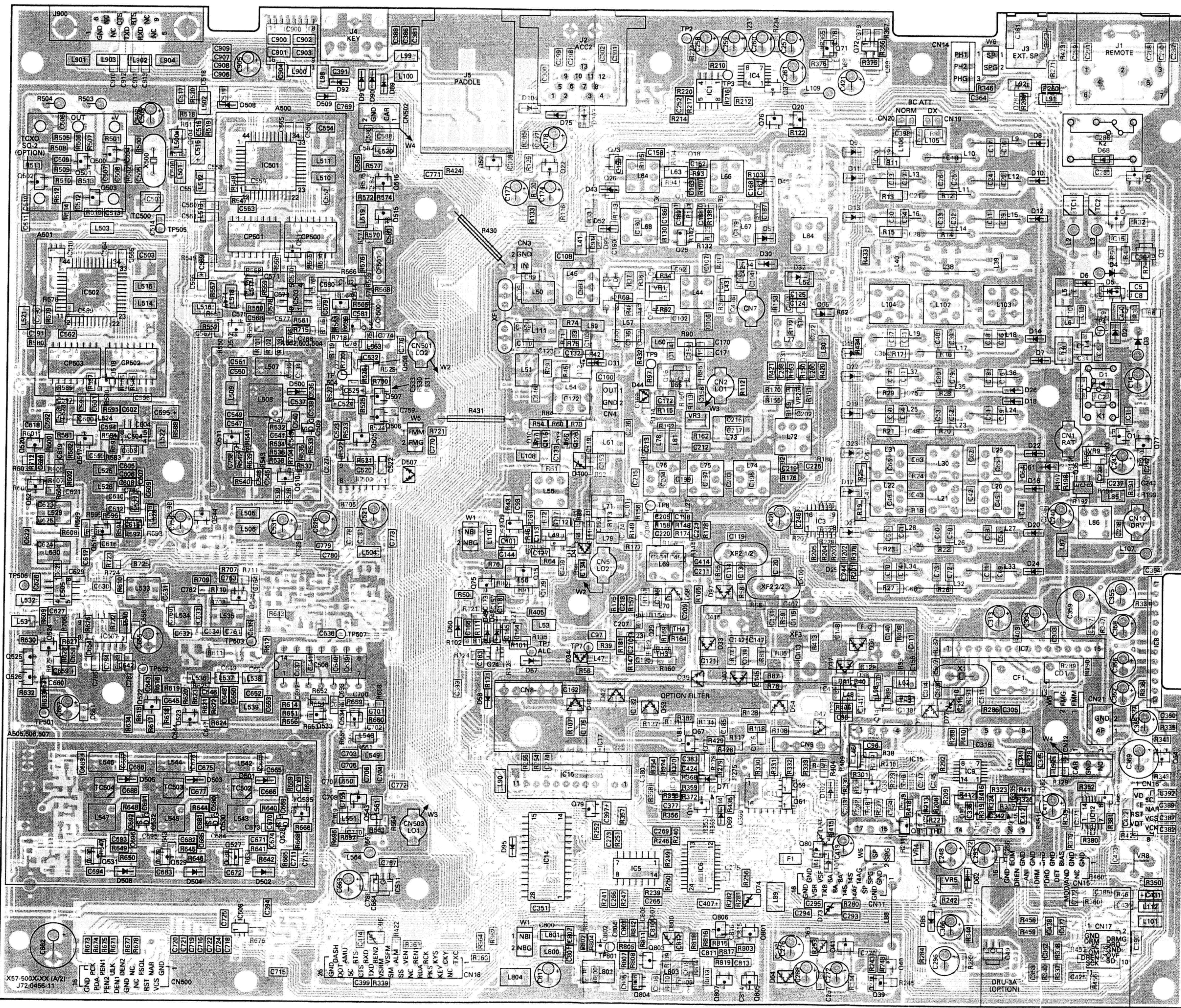
CONTROL UNIT (X53-369X-XX) 0-10 : K 0-21 : M2 2-71 : E 2-72 : E2 2-73 : E3


CIRCUIT DIAGRAM TS-570D



TS-570D PC BOARD VIEWS

TX-RX UNIT (X57-500X-XX) (A/2) Component side view 0-10 : K,M2 2-71 : E,E2,E3



K

L

M

N

O

P

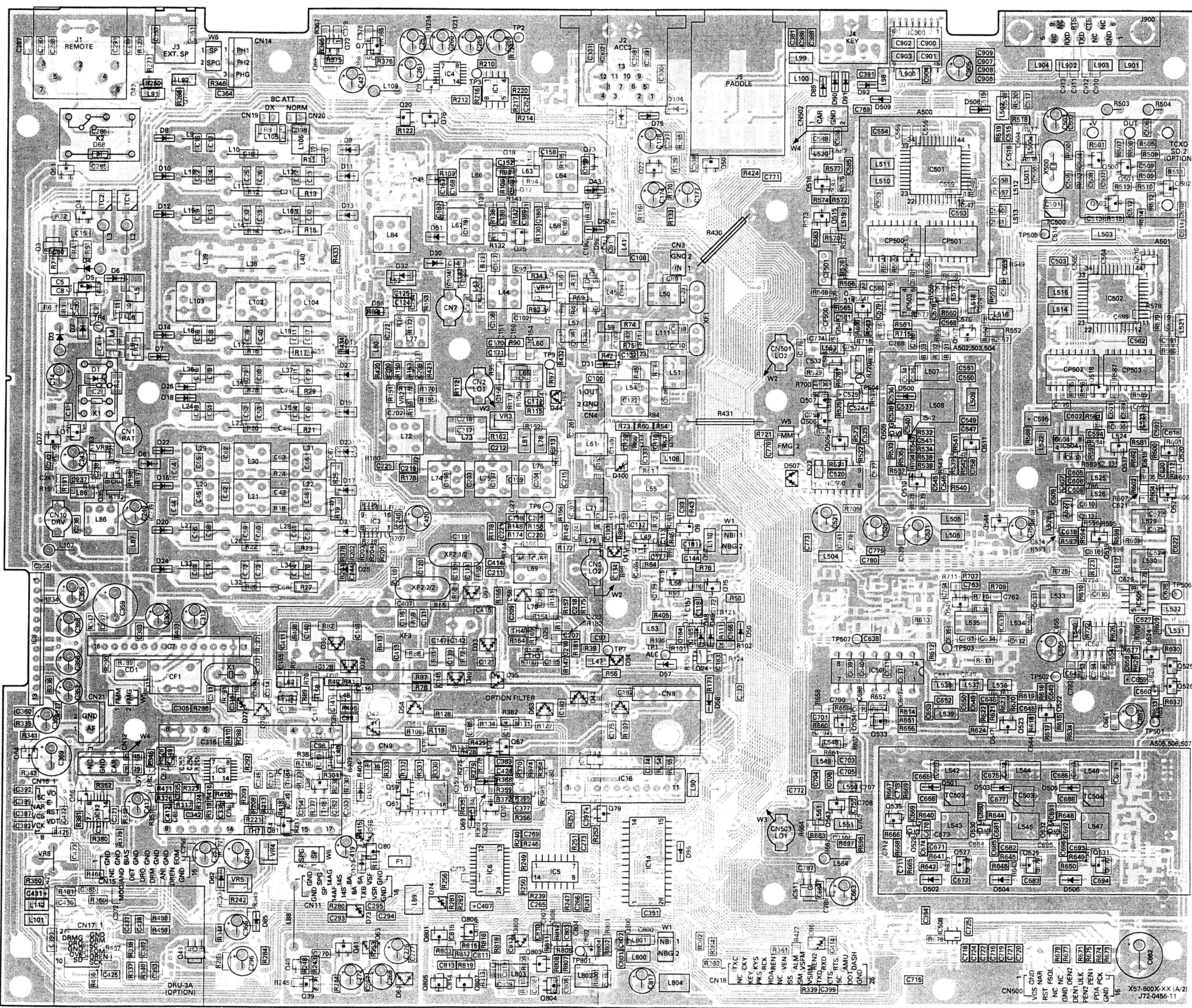
Q

R

S


T

TX-RX UNIT (X57-500X-XX) (A/2) Foil side view 0-10 : K,M2 2-71 : E,E2,E3



Component side
Foil side

TX-RX UNIT (X57-500X-XX) : RF 0-10 : K,M2 2-71 : E,E2,E3



D1, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27
 30, 32, 38, 39, 45, 51, 55,
 61, 68, 82, 103, 104 :LFB01
 D2, 5 :RLS245
 D3, 4 :V08(G)

D6-8, 10, 12, 14, 16, 18,
20, 22, 24, 26, 43, 52 :RN731H
D31, 48-50, 58, 75, 85, 89,
90-92, 95, 101, 102 :MA110 or 1S

D33. 35-37, 40, 42, 46, 47, 53, 55
D34. 41, 44
D56
D57

97:DAP236K D62, 69, 71 :RE
:ISS312 D63, 76 :IS
:RN739D D64, 77 :02
:B30-2001-05 D73 :02


51H	D74	:02CZ4. 7(Y)
226	D96	:02CZ5. 1(Y)
Z6. 2(Y)	D98	:DAN202K
Z3. 3(Z)	D99. 100	:02CZ24(Y)

Q1. 20	:	DTA124EK	Q5
Q2	:	2SD1757K(S)	Q9
Q3. 42, 68, 69	:	2SB1188(Q, R)	Q1
Q4. 51	:	DTC143TK	Q1

. 17. 18	: 2SK520 (K44)	Q14. 1
	: RU201	Q16
13	: 2SK520 (K43)	Q24
12. 25. 27. 29. 30	: 3SK131 (M)	Q26. 7

21, 22, 36, 38, 40, 41, 64 : 2S
: 2S
: FM
: DT

CIRCUIT DIAGRAM TS-570D



15, 21, 22, 36, 38, 40, 41, 64 : 2SC2412K(S)
: 2SC3357
: FMC2
. 73 : DTA143EK

Q28, 31 : 3SK184 (R) Q39

Q35 :2SC2954 Q49
Q33 52 53 65 63 Q52 82

Q37. 50, 57, 65-67.
70, 75-79, 81 : DTC 114EK
Q52. 80
Q59. 64

:2SA1037K(R) Q71 :DTC143EK IC

:2SD1624(S) Q72 :FMG3A :IC3
:DTG1215K :IC1

DIC124ER
FMA5

: NJM2904M 1C5 : NJM2902M

UPC1037GR IC6 M62363FP
BU2080ES IC7 KCD10

12 : BU4066BCFV IC8 : LA4446

ANSWER

ICII TC9174F IC16
IC14 IN113218G IC17

IC14 : KCD11


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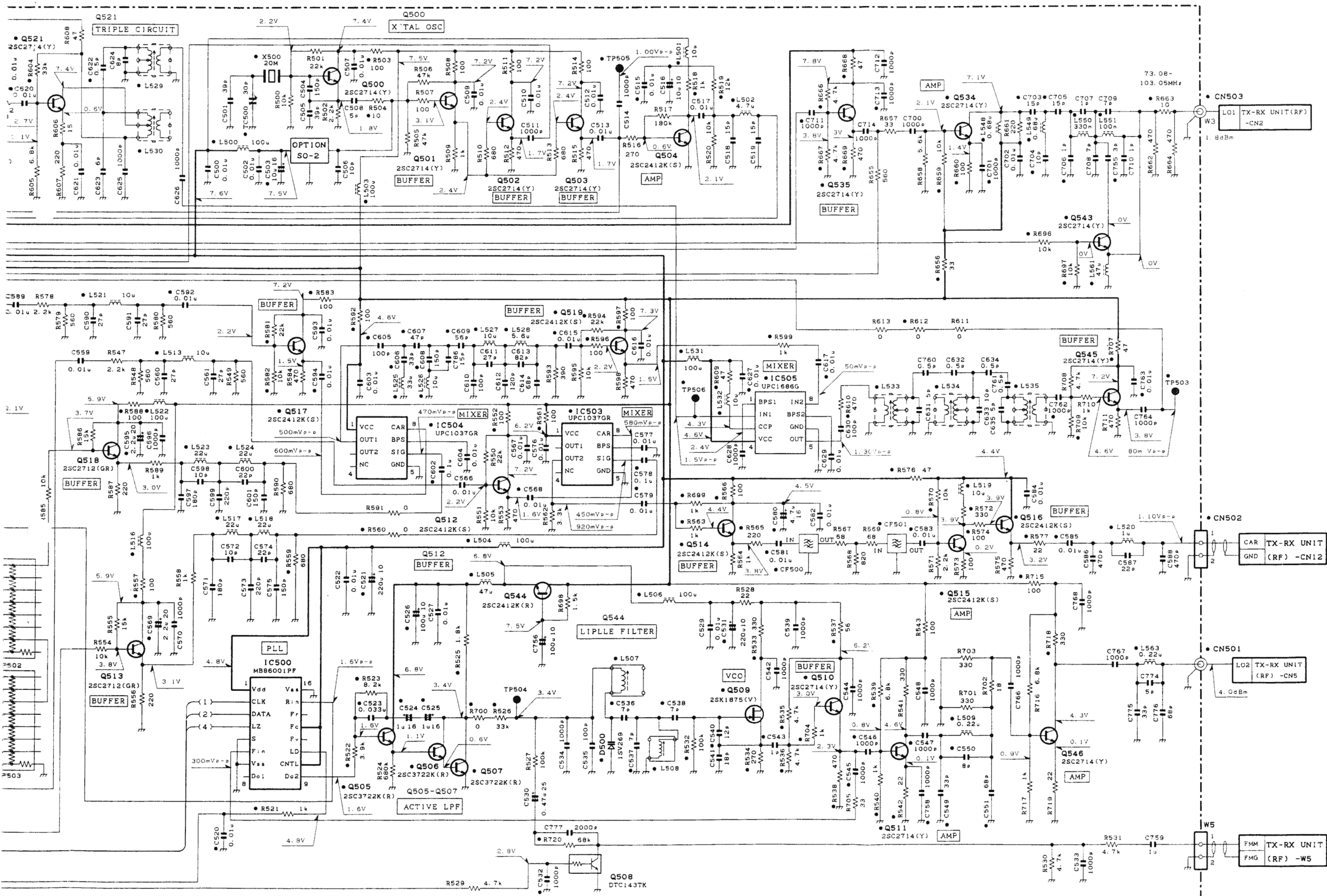
CC611
C7SOBE

[View Details](#)

TS-570D CIRCUIT DIAGRAM

TX-RX UNIT (X57-500X-XX) : PLL 0-10 : K,M2 2-71 : E,E2,E3

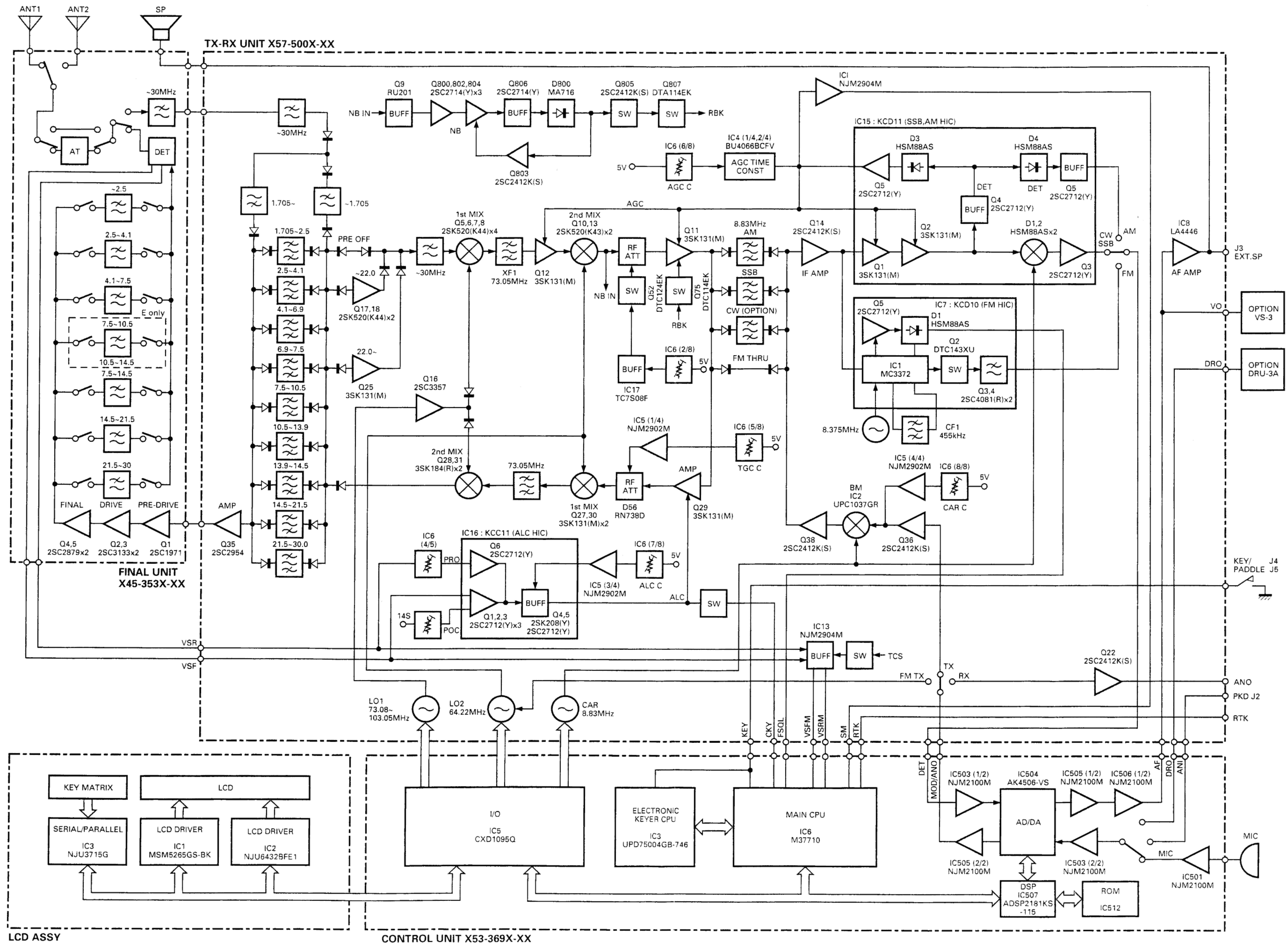




- 507	:MB86001PF	IC505	:UPC1686G	IC510	:TC7S08F
- 502	:F71022	IC506	:SN76514N	IC511	:NJM78L08UA
- 504	:UPC1037GR	IC508	:BU4S66	IC900	:ADM232LAR

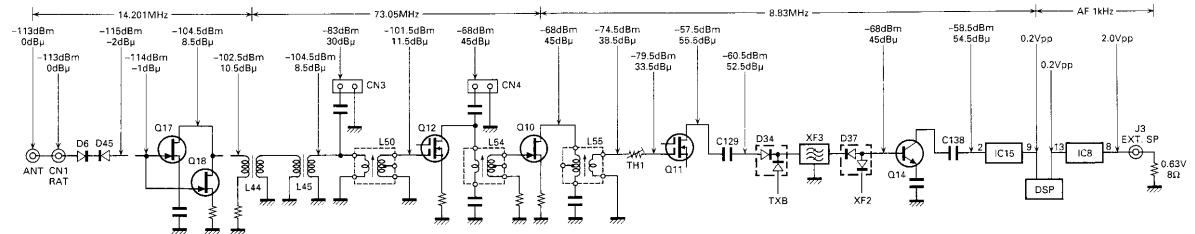
TS-570D TS-570D

BLOCK DIAGRAM



TS-570D TS-570D LEVEL DIAGRAM

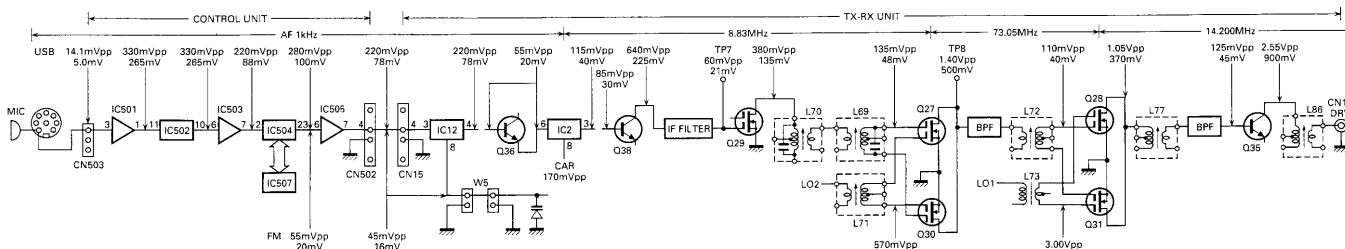
Receiver Section



Measurement condition
 Frequency : 14.200MHz
 PRE AMP : ON
 ANT input : +13dBm
 AF output : 0.63V/B_Q, 1kHz

The figures shown are signal generator output required for a constant audio output with a constant AF gain control setting.
 Set the AF gain control for 0.63V/B_Q audio output at -113dBm
 To measure signal generator output connect a 0.01μF capacitor between the signal generator and the check point.

Transmitter Section



■ Measurement condition

MIC Input : 1kHz/5mV
 PWR : 100W
 MIC level : ALC zone maximum
 Audio frequency section is measured by the AF voltmeter or Oscilloscope.
 Radio frequency section is measured by the RF voltmeter or Oscilloscope.

